Accumulated Body MOSFET with Extreme Electrostatic Threshold Voltage Tunability

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As CMOS device dimensions shrink threshold voltage (V_t) control, random dopant effects and short channel effects become increasingly important and limit device scaling. Scaling of the device width below 20 nm allows electrostatic control of the active area of a MOSFET from the two sides. In the presented device design, additional gate electrodes on the two-sides are integrated as a part of the shallow trench isolation scheme to an otherwise planar nFET. These side-gates are isolated from the active are by 18 nm of Si_3N_4 and are connected together, surrounding the active area [1]. Ultra-narrow channel devices are fabricated along with wider devices, achieving larger current drives, on the same bulk Si platform, using optical lithography.

The effective width of the presented device is estimated to be approximately 7 nm. With the application of a large negative side-gate bias, the side interfaces are accumulated with holes. This is manifested as accumulation of the whole body of the structure for the given W_{eff} which results in significant change in the depletion depth under the gate of the FET. The change in V_t follows a $\sqrt{-V_{side}}$ trend, suggesting that the effect of the accumulated charges under the gate is similar to body doping. However the deviations from this trend, as seen in $\delta V_t/\delta V_{side}$ data, suggest that there are also confinement effects taking part.

The V_t sensitivity achieved by accumulated body operation far exceeds V_t tuning achieved in double-gate transistors where the two parallel gates straddle the Si body [2].

This approach allows electrostatic V_t control, which can also eliminate the need for channel doping, hence the limitations due to random dopant effects. This multi input MOSFET allows operations such as amplitude modulation or RF filtering in a single active device for analog applications and can also serve as an AND-gate for logic applications.

[1] A. Gokirmak, S. Tiwari, *IEE Elect. Lett.* vol. 41, pp. 157-158, Feb. 2005

[2] Y. X. Liu, M. Masahara, K. Ishii, T. Sekigawa, H. Takashima, H. Yamauchi, E. Suzuki, IEEE Electron Device Lett., 25, 7, 510-512 (2004)

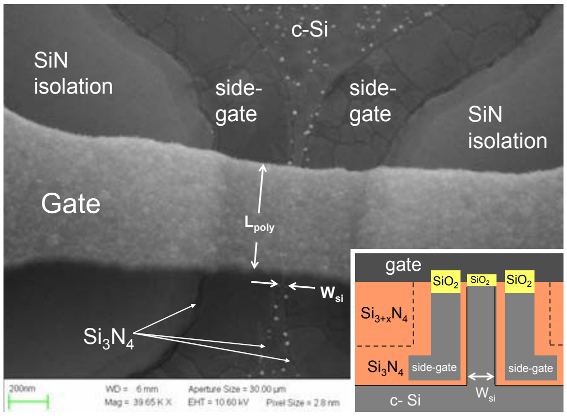

Figure 1 SEM image of a side-gated FET and cross-section schematics (inset). $t_{ox} = 4$ nm.

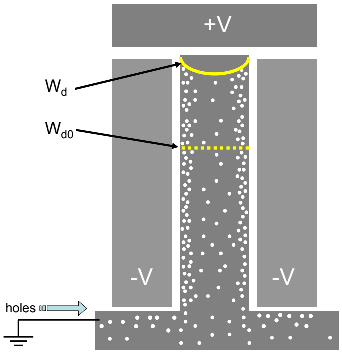

Figure 2 Cross-section schematics of operation: In an ultra-narrow channel device depletion depth is reduced to W_d due to accumulation of the body with holes when a large negative V_{side} is applied. W_{d0} is the depletion depth for a wide device.

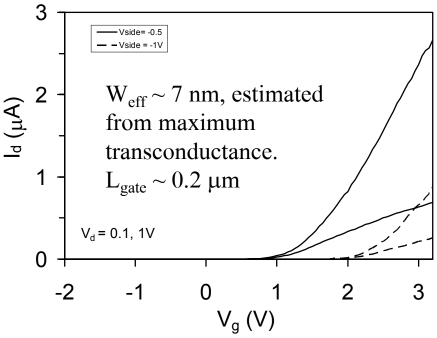

Figure 3 Transfer characteristics for $V_{side} = -0.5$ V, -1.5 V and $V_d = 0.1$ V, 1 V, in linear scale.

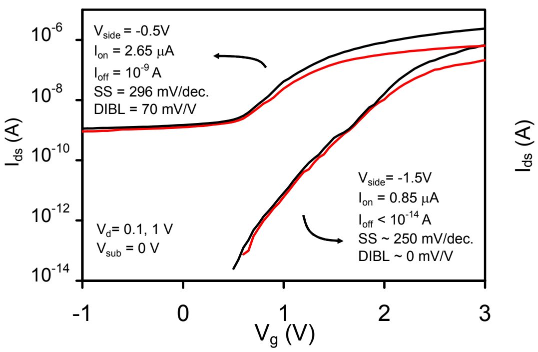

Figure 4 Transfer characteristics for $V_{side} = -0.5$ V, -1.5 V and $V_d = 0.1$ V, 1 V. $V_{sub} = 0$ V

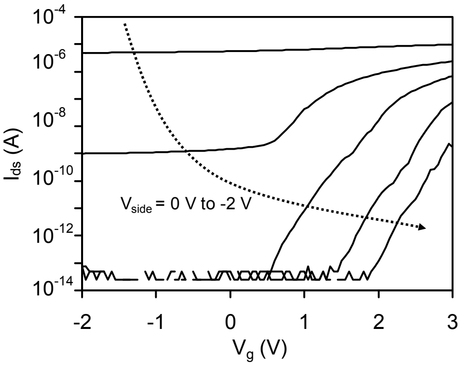

Figure 5 Transfer characteristics for $V_{side} = 0$ to -2 V, $V_{sub} = 0$ V, $V_d = 1$ V

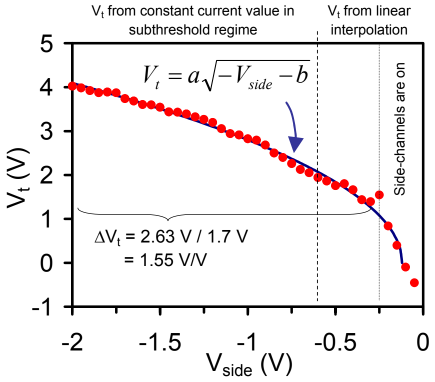

Figure 6 Threshold voltage response to V_{side} and a square root trend line.

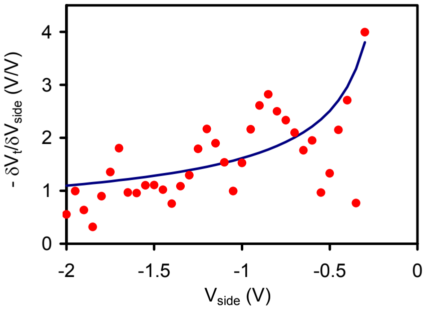

Figure 7 First derivatives of smoothed V_t versus V_{side} and the square root trend line in Figure 6.

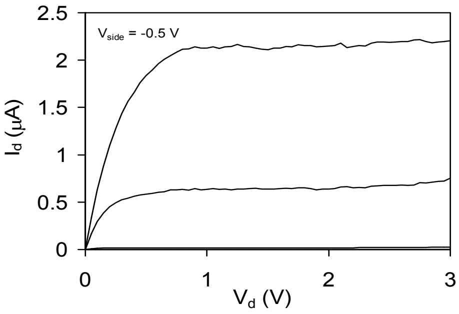

Figure 8 Output characteristics for $V_{sub} = 0$ V, $V_g = 0$ to 3 V, 1 V steps.

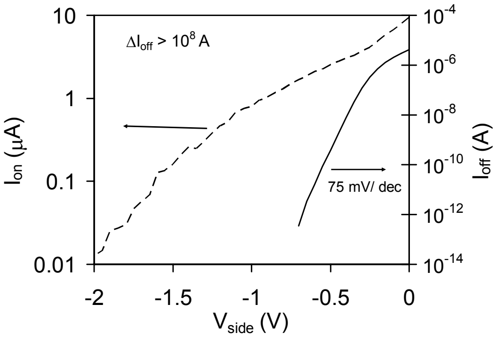

Figure 9 Maximum and minimum current levels for different V_{side}. $V_d = 1$ V, $V_{sub} = 0$ V, -2 V $< V_g < 3.2$ V.

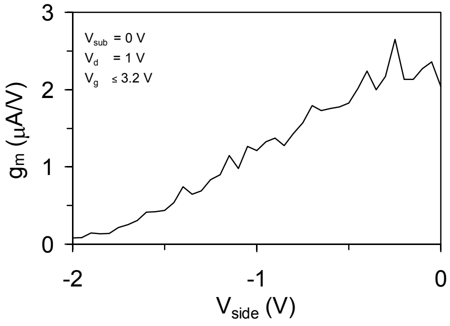

Figure 10 Maximum transconductance for $V_d = 1$ V, $V_{sub} = 0$ V, -2 V $< V_g < 3.2$ V.

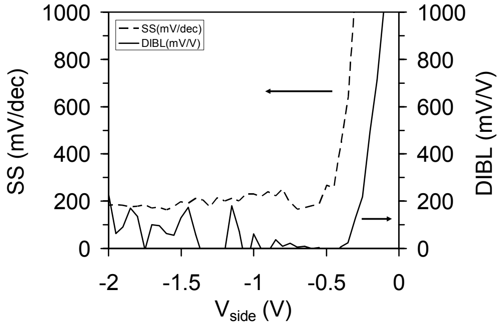

Figure 11 Minimum subthreshold slope and drain induced barrier lowering for $V_d = 1$ V, $V_{sub} = 0$ V, -2 V $< V_g < 3.2$ V.

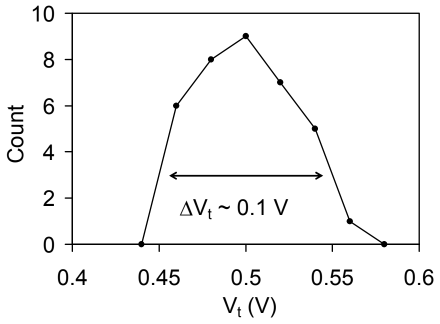

Figure 12 Threshold voltage variation in repeated measurements.