High Breakdown Voltage GaN HFETs on Sapphire Substrate

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GaN heterostructure field-effect transistors (HFETs) are very attractive for high power switching applications because they have the high electron mobility in the channel and the high breakdown field, yielding both low specific on-resistance ($AR_{DS(ON)}$) and high breakdown voltage (BV). In this paper, GaN HFETs with a very high BV over 1100V and low $AR_{DS(ON)}$ of 4.2 mΩ-cm^2 are presented, and the dependency of the device characteristics on different lengths of gate-drain spacing (L_{gd}) is fully investigated.

Fig. 1 shows the cross-sectional view of the fabricated GaN HFETs. GaN-based heterostructures were grown on 2-in c-plane sapphire substrates in Velox Semiconductor Corporation. The fabrication of GaN HFETs began with evaporated Ti/Al/Mo/Au ohmic contact metallization followed by rapid thermal annealing (RTA) at 800 ^{o}C for 30 sec under N_2 atmosphere. The contact resistance was 0.44 Ω-mm with the sheet resistance of 500 Ω/□. After ohmic formation, the mesa isolation was performed by reactive ion etching (RIE) with chlorine-based gas mixture. Thereafter, a 0.4 μm thick oxide layer was deposited on the mesa-etched region, in order to suppress pad-to-pad leakage currents through the C-doped GaN buffer. The Ni/Pt/Au gate metal was evaporated, which was followed by RTA at 500 ^{o}C for 90 sec under N_2 atmosphere. Finally, a 0.5 μm thick oxide layer was deposited only on the device active edge area, especially gate pad-to-drain ohmic contact and drain pad-to-gate metal. This layer is for protecting high voltage GaN HFETs from a sudden arcing phenomenon that may happen near the device active edge area during off-state high BV measurements. Fabricated two-finger devices with source-gate spacing of 1.5 μm, gate length of 1.5 μm and gate width of 500 μm were prepared, and gate-drain spacings (L_{gd}) were varied. Fig. 2 shows the I–V characteristics of the fabricated GaN HFETs. From fig. 2(a), The fabricated devices showed excellent pinch-off characteristics (about – 4.5 V) and maximum drain current densities (I_{max}) were 280 and 265 mA under V_{GS} = 0 V for L_{gd} = 13 and 16 μm respectively. In addition, maximum transconductance ($g_{m, max}$) of 115 mS was obtained under the drain-source voltage (V_{DS}) of 5 V and there was no significant difference of $g_{m, max}$ with the variation of L_{gd}. From fig. 2(b), record BV over 1100V was obtained on an arcing-protected HFET with L_{gd} = 16 μm and the device with L_{gd} = 13 μm exhibited the hard breakdown behavior near 620 V. In addition, a fluorinert was applied on the surface of the fabricated devices for breakdown measurements and breakdown measurement using a higher drain voltage than 1100 V could not be carried out due to measurement equipment limitations. Fig. 3 illustrates the dependency of BV, $AR_{DS(ON)}$ and I_{max} on different values of L_{gd} for the fabricated GaN HFETs. It was shown that the L_{gd} has a strong effect on the drain current slope in the linear region while no significant change in I_{max} was observed with the variation of L_{gd}. This slope is closely related to $AR_{DS(ON)}$ which is a critical parameter determining the device power loss. Here, device active area (A) was defined by the mesa isolation process. The $AR_{DS(ON)}$ increased almost linearly with increasing L_{gd} and the $AR_{DS(ON)}$ of 4.2 mΩ-cm^2 was obtained from L_{gd} = 16 μm. It was also observed that BV increased with increasing L_{gd}, suggesting the gate-drain breakdown determines the source-drain breakdown. Fig. 4 presents the BV–$AR_{DS(ON)}$ performance for the fabricated GaN HFETs with L_{gd} of 7, 10, 13 and 16 μm. The trend of BV–$AR_{DS(ON)}$ showed a clearly linear relation, suggesting that the device performance is very predictable with the variation of L_{gd}. For L_{gd} = 16 μm, a BV over 1100 V and $AR_{DS(ON)}$ of 4.2 mΩ-cm^2 was achieved from the fabricated HV GaN HFET, even approaching the SiC limit.

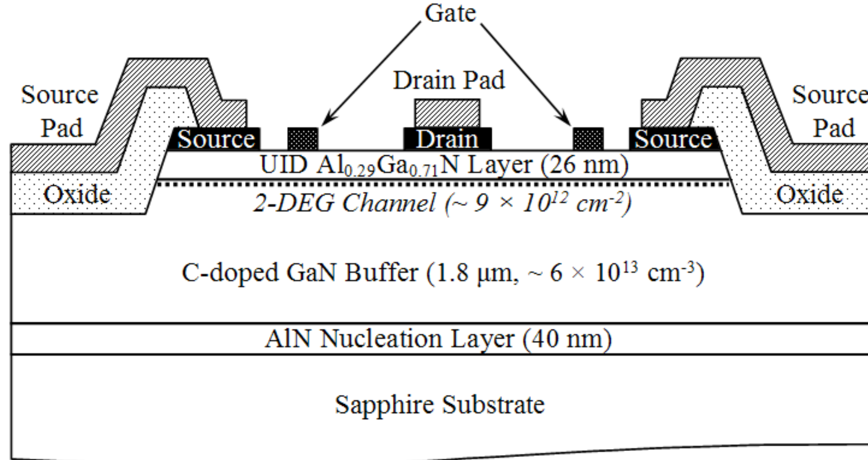

Fig. 1 Cross-sectional structure of the fabricated high voltage GaN HFETs

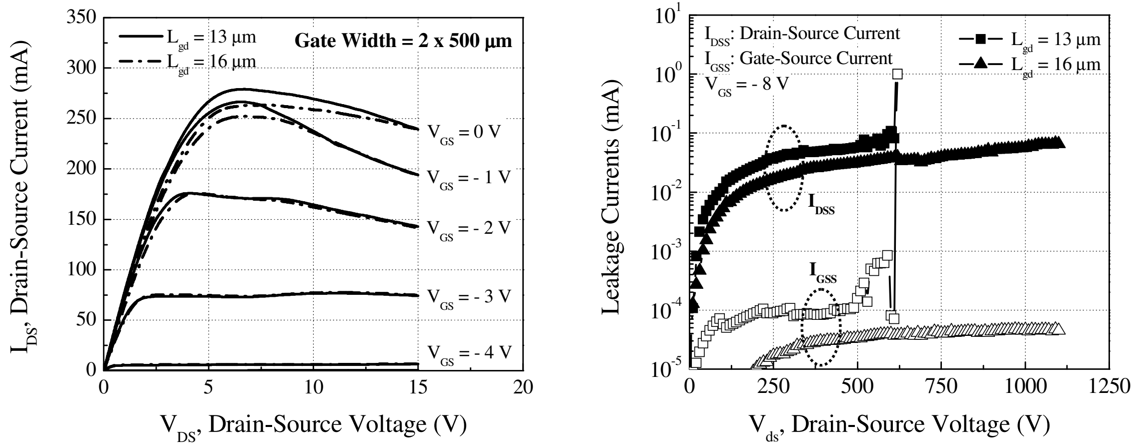

Fig. 2 I–V characteristics of the fabricated high voltage GaN HFETs (a) On-state (b) Off-state

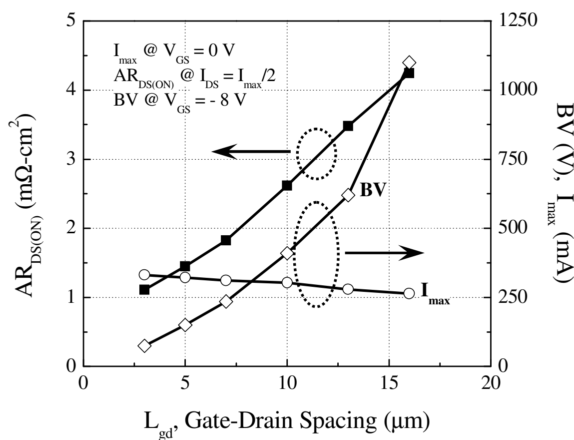

Fig. 3 Dependency of BV, I_{max} and $AR_{DS(ON)}$ on different lengths of L_{gd}

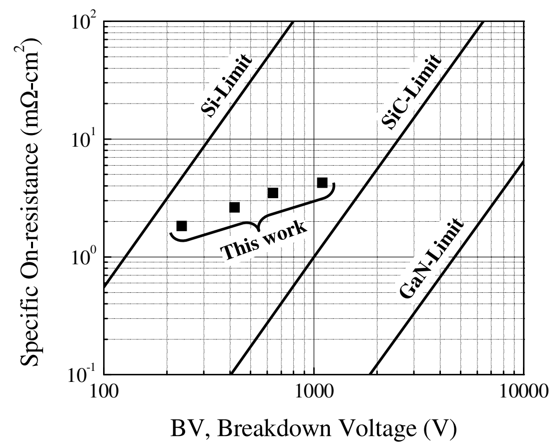

Fig. 4 BV–$AR_{DS(ON)}$ performance for the fabricated devices