High-Yield Silicon Carbide *Vertical Junction Field Effect Transistor* Manufacturing for RF Applications

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Abstract

Silicon Carbide (SiC) is ideally suited for high-frequency applications due to its high critical field strength, its high saturated drift velocity, its relatively low dielectric constant, and its high thermal conductivity. Silicon Carbide *p*+ ion-implanted vertical junction field effect transistors (VJFETs) have been manufactured for high-frequency applications. Low resistance and capacitance considerations set the high-frequency VJFET drift layer thickness in the 2.5 to 3.5 μm range. A cross section schematic of the VJFET structure is shown in Figure 1. In the on-state, majority carriers (electrons) flow vertically from source to drain. To control the current through the device a voltage is applied to the gates, which adjusts the width of the depletion regions between the p-type gates and the n-type channel.

The epitaxial parameters, processing, and design have been optimized for high yield manufacturing, reliability under extreme conditions, fast cycle times, and high volume. Self-aligned processing and high resolution lithography enable sub-micron linewidths and uniform metallizations. Dielectric layers provide device isolation and reliability. Precise reactive-ion-etching enables deep and vertical source-pillar sidewalls with minimal roughness (Figure 2). After implant anneal, the surfaces were passivated by sacrificial oxidation. Combinations of thermal and high-temperature densified CVD oxides were used in various stages of processing. Wet cleanings and short surface reactive-ion-etchings were performed to remove residues. As a result, well passivated surfaces were obtained as evidenced by the very low leakage currents and the very sharp onsets of reverse breakdown, shown in Figure 3.

The functional yields for the high-frequency VJFETs were in the 78-88% range, for an eight wafer lot (cf. Figure 4). Process optimizations led to excellent wafer uniformity. This is evident in the gate-to-source forward voltage and the drain-to-source resistance histograms of Figure 5.

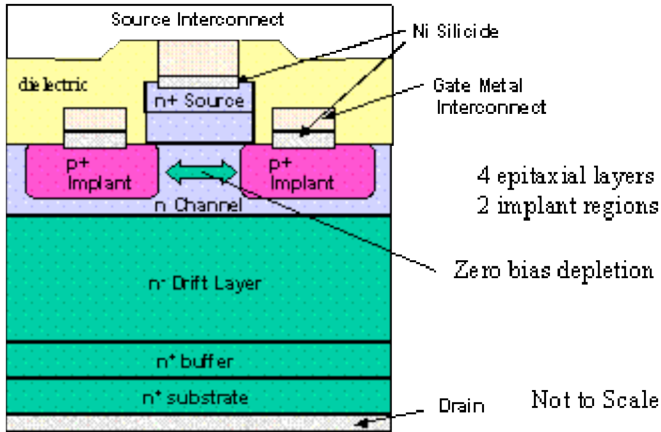

Figure 1. Cross-section schematic of a Normally-On Ion-Implanted SiC VJFET.

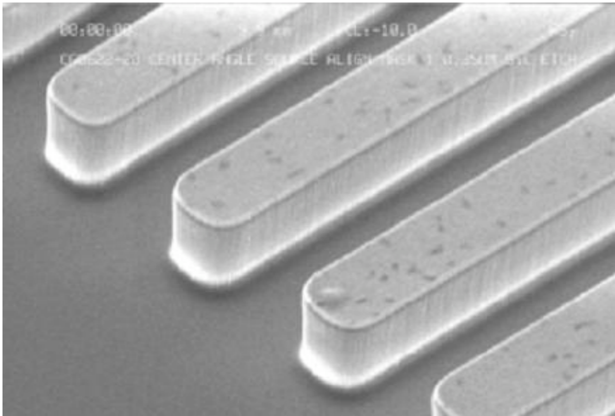

Figure 2. Precise processing enables deep and vertical sidewalls, necessary for the VJFET structure.

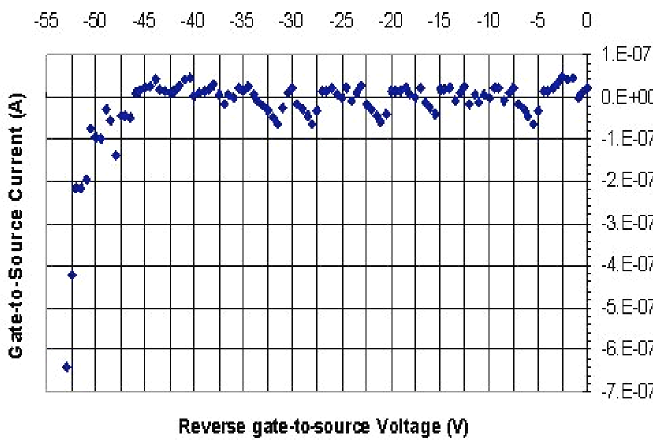

Figure 3. Low gate-to-source leakage current with sharp onset of reverse breakdown, providing low loss device operation.

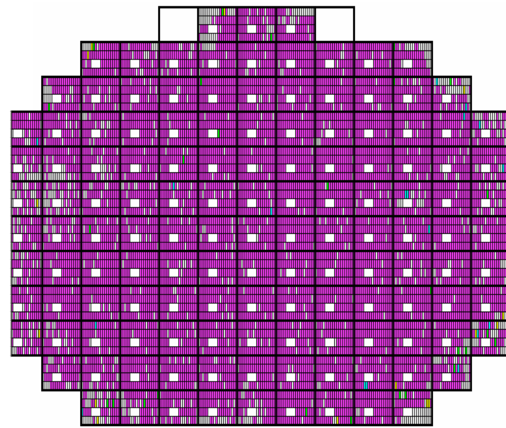

Figure 4. Gate-to-source breakdown voltage wafer map, showing outstanding device yield of 88%.

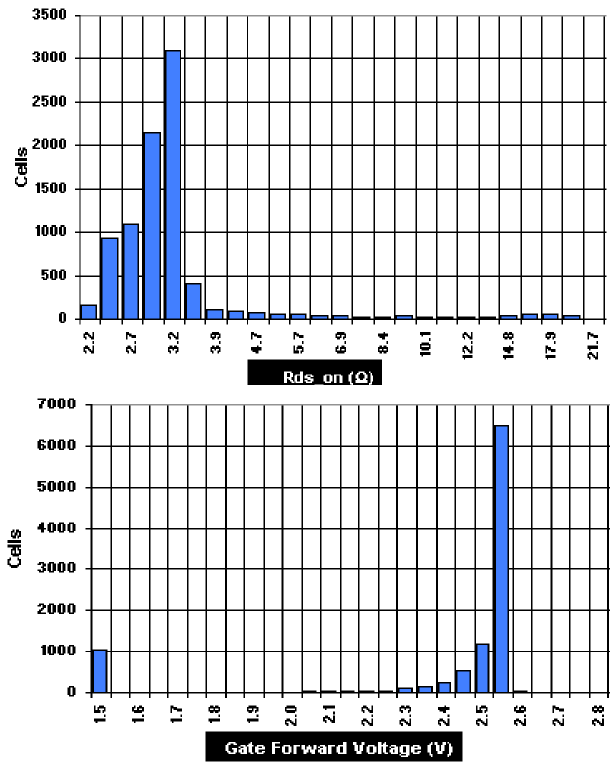

Figure 5. Gate-to-source forward voltage and drain-to-source resistance histograms, showing excellent wafer uniformity.