BULK AND INTERFACIAL DEFECTS IN HIGH-K GATE STACK: ORIGIN AND PROPERTIES

G. Bersuker, C. S. Park, J. Barnett, P. Lysaght, R. Choi, B. H. Lee, and R. Jammy
SEMATECH
2706 Montopolis Dr., Austin, TX 78741; gennadi.bersuker@sematech.org

Transition metal and rare earth oxides are among the high dielectric constant (high-k) materials currently being investigated as gate dielectrics in highly scaled transistors. A common electronic feature of these materials is the presence of d-shell states, which make their structural properties drastically different from those of the conventional SiO_2 gate dielectric. One of the consequences of the d-electron bonding in high-k dielectrics is a relatively high density of as-grown defects, which may contribute to "slow" (within seconds; see Fig. 1) and fast (in the microsecond range; see Fig. 2) reversible electron trapping processes affecting transistor threshold voltage and mobility, respectively. Based on the proposed model for the charge trapping process, we have estimated the values of energy, capture cross-section, and concentration of the electron traps. These values match those of the negatively charged oxygen vacancies (in the concentration range of about 0.5 O atomic %) obtained by the ab initio calculations for the monoclinic hafnia.

As a result of dielectric deposition and processing, high-k gate stacks usually contain SiO_2 interfacial layers (IL) between a high-k dielectric and the substrate. This IL, while increasing the total electrical thickness of the gate stack, provides a smooth interface with Si and partially screens the negative effect on the channel carrier mobility associated with fixed charges and soft optical phonons in the high-k films. However, changes in some critical electrical characteristics of the IL—in particular, an increase in its dielectric constant and fixed charge density—were observed, the magnitude of the effect being strongly dependent on the starting (pre- high-k deposition) IL thickness (see Fig. 3). It is proposed that this modification in the electrical properties is caused by the oxygen deficiency of the IL induced by the high-k dielectric via the thermodynamically favorable process of reducing the pre-existing oxygen vacancies in high-k. This suggestion is supported by the Si $L_{2,3}$ edge electron energy-loss spectroscopy (EELS) data, which shows a signature of Si atoms in various under-oxidized states in the IL after high temperature anneal (1000C), consistent with the X-ray photoelectron spectroscopy (XPS) results. The generation of oxygen vacancies can also be monitored by electron spin resonance (ESR) measurements, which show a significant increase of E' and Pb-like defect density in the IL after high-k processing.

The dominant contribution of pre-existing defects and precursor defects in the high-k gate stacks to instability in the electrical characteristics of high-k devices requires re-evaluation of the reliability assessment methodologies previously established for SiO_2 gate dielectrics.

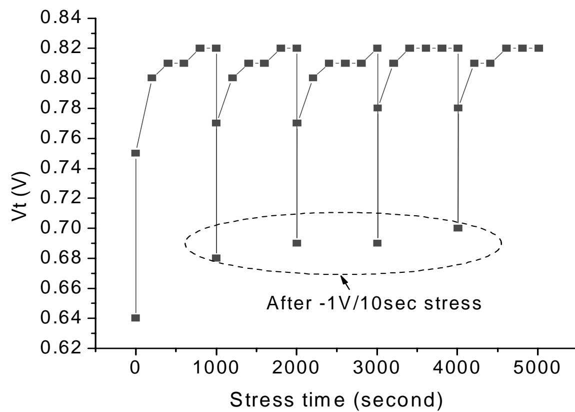

Fig. 1. Threshold voltage change in TiN/3 nm HfO_2/1 nm SiO_2 NMOS transistor during stress cycles, which include 1000-sec substrate injection stress at V_g=2.4V followed by 10-sec stress of the opposite bias (-1V).

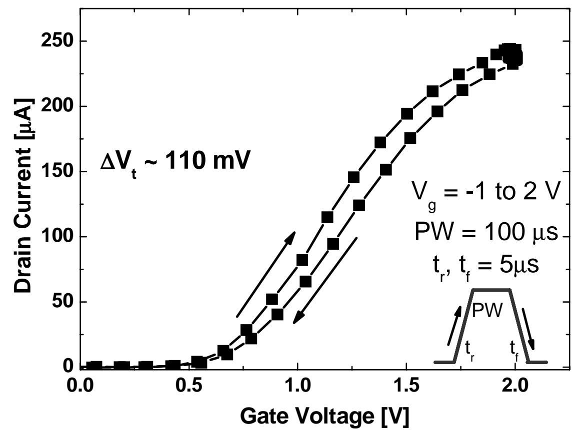

Fig. 2. Transistor I_d-V_g characteristics during the 100µs V_g pulse. The relative shift of the up and down I_d-V_g curves defines the change of threshold voltage (ΔV_t) caused by electron trapping.

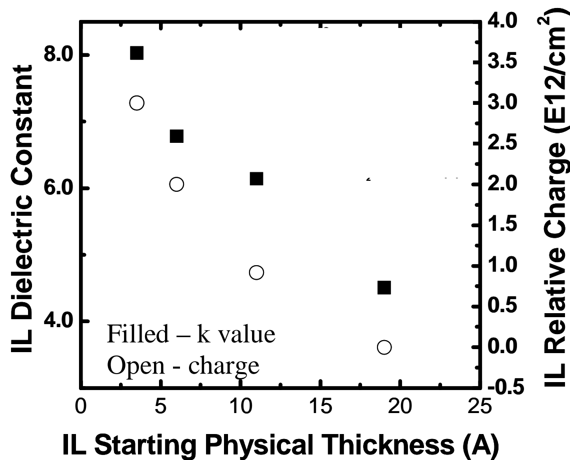

Fig. 3 Post-processed IL dielectric constant and fixed interface charge (relative to reference sample of the thickest interfacial layer) vs. thickness of starting IL.