Present Status and Future Directions for SiGe HBT Technology

Marwan H. Khater *et al.*

IBM T. J. Watson Research Center, Yorktown Heights, NY 10598
Phone: 914-945-2076, Email: mkhater@us.ibm.com

Abstract

Recent developments in SiGe HBT transistor technology achieved operation speeds approaching 400 GHz [1-5] and enabled circuits operation at 60 GHz [6]. Vertical scaling and impurity-profile engineering of the collector and SiGe base, enabled by modern epitaxial growth techniques, allowed SiGe HBTs to operate at cut-off frequencies (f_T) up to 375 GHz, approaching frequencies similar to those of III-V material based HBTs [3]. The improvement in f_T, however, trades off and limits the maximum oscillation frequency (f_{MAX}) of the device due to increased parasitic capacitance and resistance caused by vertical scaling according to the approximate relation

$$f_{MAX} \approx \sqrt{\frac{f_T}{8\pi R_B C_{CB}}}$$

where, R_B is the total base resistance and C_{CB} is the collector-to-base capacitance. These parasitics can be optimized to further improve the device speed (e.g. f_{MAX}) by lateral scaling and device structure modification enabled by advanced CMOS-compatible lithography and process techniques readily available for SiGe HBTs. Lithography techniques are used to implement selectively implanted collector (SIC), which can be scaled down to reduce C_{CB} [7]. In addition, the emitter in modern SiGe HBT technology can be scaled down to sub-100 nm dimensions using advanced lithography techniques to improve the device speed and allow low power operation. However, scaling of SiGe HBTs has limitations similar to those encountered in CMOS technology. These limitations have been successfully overcome by the advancement of new materials, process techniques, and structural innovations. A significant structural improvement is the implementation of a raised extrinsic base self-aligned to the emitter, which allows reduction of R_B and C_{CB} independently [1]. In such a device structure, the spacing between the extrinsic base and the emitter is determined by a spacer formed in a similar fashion implemented in CMOS technology. Furthermore, the raised extrinsic base resistance has many components that can be optimized to further reduce R_B and improve the device speed. The first implementation of self-aligned device structure with raised extrinsic base achieved f_{MAX} of 285 GHz, with associated f_T of 207 GHz [1]. With further vertical scaling, to balance f_T and f_{MAX}, such a device structure demonstrated f_T and f_{MAX} both of which exhibiting 300 GHz [4]. Another improvement in the device structure is reducing the spacing between the extrinsic base silicide and the emitter to reduce R_B, which achieved f_{MAX} of 350 GHz without affecting f_T of 300 GHz [5]. Other structure modifications showed C_{CB} reduction through new collector construction [8] and emitter resistance (R_E) reduction, as well as breakdown voltage (BV_{CEO}) increase, by implementing metal emitter [9].

In this work, the state of the art of SiGe HBTs will be reviewed with emphasis on materials and process techniques enabling the device performance improvement. In addition, challenges of new process technologies and materials implementation to improve SiGe HBTs performance beyond 350 GHz will be discussed.

[1] B. Jagannathan *et al.*, *IEEE Elec. Dev. Lett.* **23**, p. 258 (2002).
[2]J.-S. Rieh *et al.*, *IEDM Tech. Dig.*, p. 771 (2002).
[3] J.-S. Rieh *et al.*, *Proc. of IPRM*, p. 374 (2003).
[4] J. -S. Rieh *et al.*, *IEEE RFIC Symp. Dig.*, p. 395 (2004).
[5] M. Khater *et al., IEDM Tech. Dig.*, p. 247 (2004).
[6] B. Floyd *et al.*, *IEEE J. Solid-State Circuits* **40**, p. 156 (2005)
[7] A. Stricker *et al.*, *Mat. Sci. Semi. Proc.* 8, p. 295 (2005).
[8] B. Heinemann *et al., IEDM Tech. Dig.*, p. 251 (2004).
[9] J. Donkers *et al., IEDM Tech. Dig.*, p. 243 (2004).