InP DHBT Technology for High Frequency Analog and Digital ICs

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The InP/InGaAs/InP heterojunction bipolar transistor (DHBT) has inherent material advantages over a SiGe HBT (higher carrier mobilities and saturated velocities, higher breakdown voltage for InP collector), however, silicon manufacturing processes enable deep submicron scaling of transistor junction dimensions and aggressive scaling of extrinsic parasitics. Recent research in InP HBTs has focused on submicron device scaling. If properly scaled, InP HBTs with 0.5 μm emitter junction widths demonstrate simultaneous RF figures merit f_t and f_{max} >400GHz while maintaining a >4V breakdown voltage. A key challenge faced when scaling the transistor has been maintaining and improving device yield and manufacturability. Typical III-V fabrication processes, such as self-aligned evaporation and liftoff, are not amenable to high levels of yield, particularly as feature sizes are scaled to submicron dimensions. Therefore, silicon-like fabrication techniques are being developed and incorporated into InP HBT process flows.

Self-alignment of the emitter and base contact is critical to minimizing the base-collector capacitance and base resistance of the HBT. We have developed an InP HBT technology that utilizes dielectric sidewall spacers and electroplated contacts to form a self-aligned base-emitter junction. The process is scalable to emitter dimensions <100nm while maintaining high levels of yield. In this process, the base metallization is *selectively* electro-deposited directly on the base semiconductor and electrically isolated from the emitter by a dielectric sidewall spacer. Similar to a silicon salicide process, this method of forming self-aligned III-V contacts has potential applications for a wide range of electron devices.

The HBT technology has been used to fabricate a variety of mixed-signal ICs ranging from a frequency divider operating at 150GHz (~50 HBTs) to a direct digital synthesizer operating at >10 GHz (~5000 HBTs). In this talk, device and circuit results from the technology will be presented, and methods for further parasitic reduction involving ion implantation and regrowth will be discussed.

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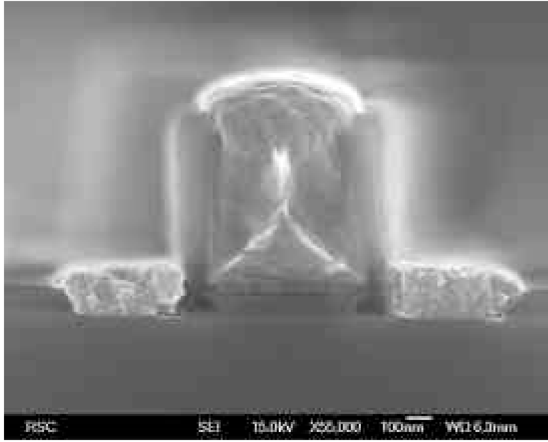

Fig.1: SEM cross-section of self-aligned base-emitter junction formed with electroplating processes

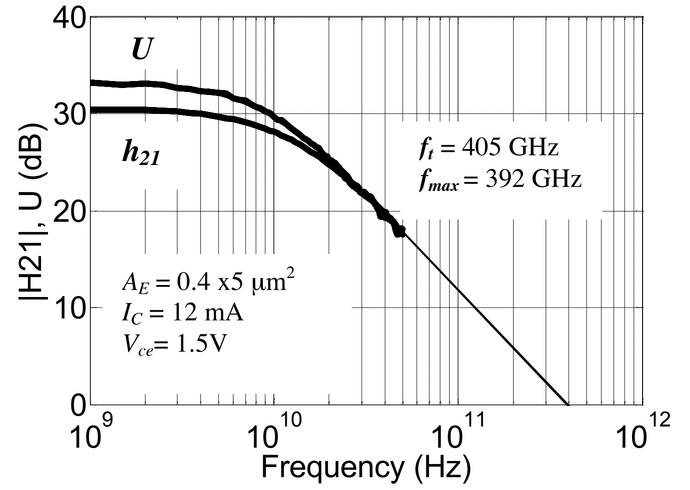

Fig. 2: RF gains of submicron InP HBT

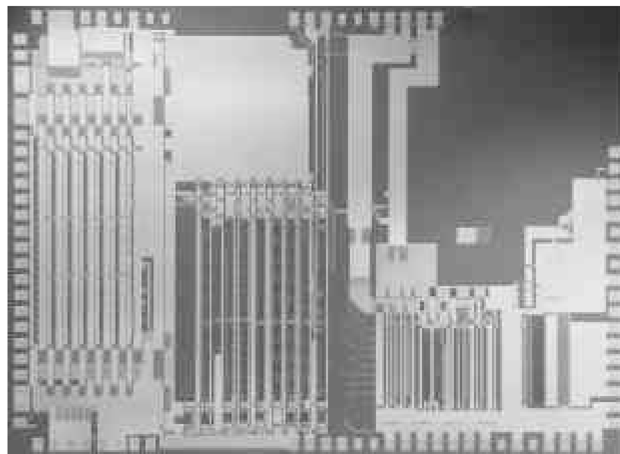

Fig.3: Chip photograph of 5000 transistor direct digital synthesizer (DDS).