Selected Electron Device Research Projects at Cornell University

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Projects on wide band gap semiconductors for microwave power amplification include short-gate (0.1 – 0.5 micron) AlGaN/GaN HEMT's, and SiC MESFET's and HEMT's. The goal is to raise the figure of merit ($Pf_t^2 \cdot Z_{load}$), by materials, processing and layout design optimization. The GaN HEMT's are being studied with sapphire, GaN, AlN, Si and SiC substrates. Effort on lowering the contact transfer resistance, lowering the bulk Si_3N_4 passivation conductance, and reaching high breakdown voltage, using gate field plates, are included. Improved electron transit velocity in GaN channels by lowering the electron and phonon densities is being studied. Long gate lengths (1.5 – 2.5 microns) GaN HEMT's are being studied for power switching applications. A combination of very high breakdown voltage and very low on resistance is improved, using a source-connected field plate. High power SiC MESFET's for microwave applications, and recently, SiC HEMT's for microwave power amplifications are being studied. The latter are made possible by using a heterojunction of SiC polytypes. Using ultra short GaN (300 and 600Å) high field drift spaces, with an AlGaN heterojunction ballistic electron launcher, negative effective mass electrons can allow negative differential conductivity up to THz. 0.25 micron n-type GaN drift regions are being studied to differentiate between electron transfer to upper valleys and electron slow-down due to LO phonon buildup in these THz negative differential conductivity devices. Following the discovery of initial small band gap (0.65V) InN, grown by MBE, InGaN solar cells capable of efficient operation anywhere in the solar spectrum, are now under study. Materials growth of AlGaN/GaN for HEMT's has been carried out by OMVPE in cooperation with industry, and by MBE. The THz devices are being grown by MBE. VPE of SiC is used for MESFET's and HEMT's, following the discovery of 2DEG at the polytype heterojunction, is being carried out.

The issues in silicon electronics today are those related to complexity — the hierarchy of scales in time and length, and issues of energy and power dissipation that arise in large systems. Because electronics is based on the charge transport and change in the electromagnetic fields, non-linearity and collective effects are increasingly important issues at the smallest length scales while signal delays are important at the integrated system scale. Small dimensions also result in increasing power density in ever smaller volumes. At the device level, an important approach to controlling power and achieving devices with high non-linearity is the use of the double-gate or back-gated structures where threshold voltage can be dynamically modified and charge transport is restricted to ultra-thin channels of 10's of nm. At the system level, the delay and architectural issues can be selectively addressed through three-dimensional integration. Experimental and theoretical results from these two approaches will be shown to address silicon electronics operation at 10-20 nm gate lengths and x10 levels of integration than what can currently be imagined using planar and newer technologies.

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