A Comparison of N+ type and P+ type Polysilicon Gate in High Speed Non-Volatile Memories

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Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) [1] and nano-crystal memory [2] have been considered as a replacement floating gate memory due to simple process, low voltage operation and high speed. In the SONOS memory, an ultra-thin oxide-nitride-oxide (ONO) film with high trap density and strong localization of the trapping provides the scalability and retention. This may allow longer retention with thinner tunneling dielectrics, leading to lower operating voltages. However for the high speed performance, SONOS needs improvement in erase time - the discharging process of electrons from the traps. Thus we have speculated on the effect of electric fields in the trapping-control gate region, and characterized the effects of doping on poly-silicon gate in SONOS memory device. Our experiments compare the characteristics of SONOS memories between n+ type and p+ type polysilicon gate. Figure 1 shows the schematics of these structures. SONOS memory devices have been fabricated with 0.5 um n+ type gate or p+ type gate on SOI substrates using the conventional CMOS processing technology. The tunneling oxide of 3 nm thickness was grown at 900 C and then a Si_3N_4 film of 5.5 nm and the blocking oxide layer of 7 nm were deposited by low pressure chemical vapor deposition (LPCVD). Figure 2 shows a transmission-electron micrograph of the cross-section of this grown and deposited memory stack with the dark region as the silicon nitride. After these gate stacks process, n+ type or p+ type poly-silicon is deposited.

Using the program/erase threshold voltage window as 4 V in p+ type poly-silicon gate memory, the program time is approximately 20 us at 16 V program voltage and the erase time is about 1 ms at a –16 V erase voltage using FN tunneling method. The capture and erase characteristics also show asymmetries in the capture and erase processes due to the physical differences in the processes themselves. The capture process is based on Fowler-Nordheim injection where the relevant capture cross-section is related to the extent of the potential perturbation of the defect. This capture cross-section is one to two orders of magnitude smaller than that of silicon nanocrystals. The erasure process is presumably a Poole-Frenkel mechanism, or other similar de-trapping process with strong localization and field-dependence. The erase time of SONOS memory device is somewhat slow, and it is due to the injection of electrons through top oxide from the gate and heavy mass of holes. To solve this problem, several methods have been introduced recently. Using a high k material instead of SiO_2 thin film is useful for decreasing the transmission of electrons in the top oxide due to the capacitive coupling [3]. However, this may not be suitable technologically in a CMOS process. We expect that the higher work-function of p-type gate to improve erase speed. Figure 4 shows that the erase speed of p+ gate is much faster than that of n+ gate. The work will describe detailed experimental measurements in support of this conclusion.

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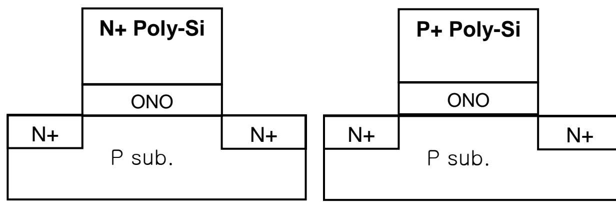
[1] M. K. Kim, S. D. Chae, H. Silva, S. Tiwari, “Ultra-short SONOS memories”,IEEE Transactions on Nanotechnology, v 3, 4, 417 - 424 (2004)

[2] S. Tiwari et al., " A silicon nanocrystals based memory", Appl. Phys. Lett. 68, pp.1377-1379, 1996

[3] Chang Hyun Lee, Kyun In Choi, Myoung Kwan Cho, Yun Helb Song, Kyu Chan Park and Kinam Kim, “A Novel SONOS Structure of SiO2/Si3N4/Al2O3/ TaN Metal Gate for Multi-Giga bit Flash Memories” IEDM 2003



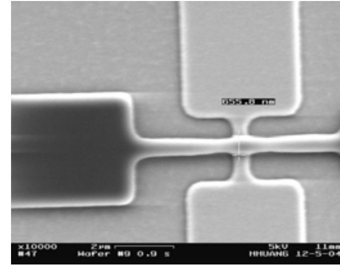


Figure 1. Schematic of n+ type gate & p+ type gate device structures and an SEM image.

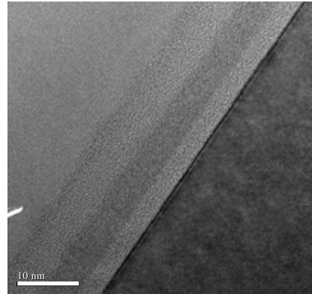


Figure 2. TEM image of ONO (3/5.5/7 nm) structure.

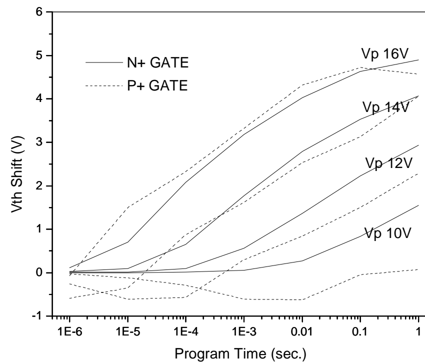


Figure 3. Programming speed characteristics of n+ and p+ gate.

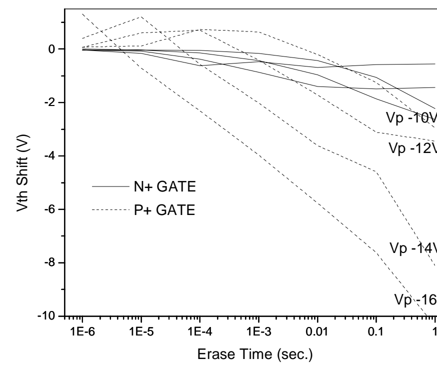
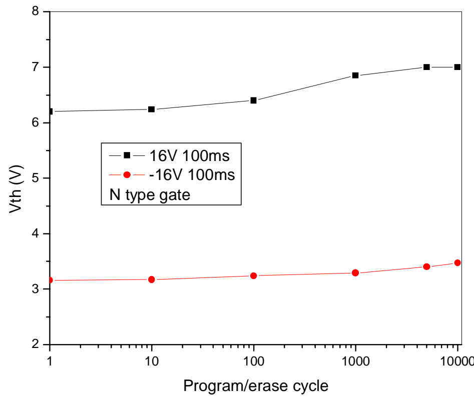


Figure 4. Erase speed characteristics of n+ and p+ gate.



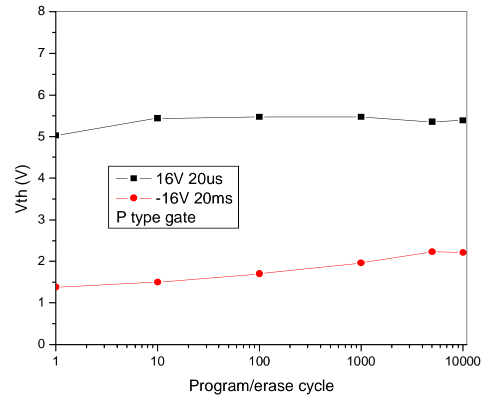


Figure 5. Endurance characteristics of n+ gate and p+ gate.