Non-Volatile High speed & Low power Charge Trapping Devices

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Obtaining non-volatile, low power and fast memories at short dimensions is a key challenge in electronics. Among the approaches being adopted are use of storage of single or few electrons such as in nano-crystal memories[1], and other modifications such as the use of silicon-oxide-nitride-oxide-silicon (SONOS) or back-floating gates[2,3].

We report the operational characteristics of ultra-small-scaled SONOS (below 50 nm gate width and length) and SiO_2/SiO_2 structural devices with 0.5 um gate width and length where trapping occurs in a very narrow region. This experiment shows the memory characteristics of the retention time, endurance cycles, and speed in SONOS and SiO_2/SiO_2 structures. Silicon nitride has many defects to hold electrons as charge storage media in SONOS memory. Defects are also incorporated during growth and deposition in device processing. Our experimens show that the interface between two oxides, one grown and one deposited, provides a remarkable media for electron storage with a smaller gate stack and thus lower operating voltage structure.

The devices have been fabricated on SOI wafers. Following the active region definition on the thinned silicon-on-oxide using sacrificial dielectric stack, the oxide-nitride-oxide stacks (3 nm/7 nm/9 nm) in SONOS and the oxide-oxide stacks (3 nm/7 nm) in SiO_2/SiO_2 are grown and deposited. Poly-silicon gate patterning and sidewall process are utilized in making the devices.

The reduction of the effective barrier by applying larger write and erase voltages causes the higher tunneling probabilities because the write and erase mechanism is Fowler-Nordheim tunneling or field assisted tunneling. This is observed in both structures as a decrease in writing and erasing times with increased applied tunneling voltages. The trap densities in both structures have been calculated with the threshold voltage shift assuming the centroid of the charge is in the middle of nitride layer in SONOS device, and at the tunnel oxide/ blocking oxide interface or in the middle of the blocking oxide layer in SiO_2/SiO_2 charge trapping device. The capture process is based on Fowler-Nordheim injection and the erasure process is most probably a Poole-Frenkel mechanism, or some other similar detrapping process with strong localization and field-dependence. This different mechanism has been studied through the activation energy of the capture and emission processes using the time-dependence of the response to write or erase voltages[4]. Nearly all of such tunneling-based injection processes that have been modeled have a characteristic bias/energy dependence that is inversely exponentially related to the thickness and barrier height. The activation energy is ~1 eV for write process and 1.5 to 2.0 eV for the erase process in SONOS device and, is ~0.45 eV for the write process and ~0.51 eV for the erase process in SiO_2/SiO_2 structural device. Details of the comparison between these charge trapping memories will be presented.

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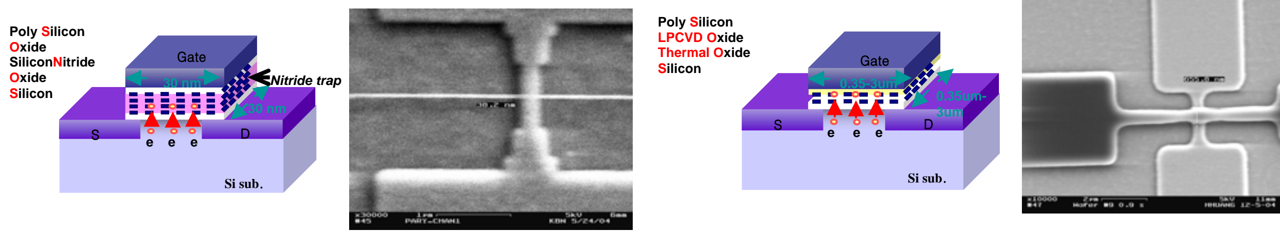
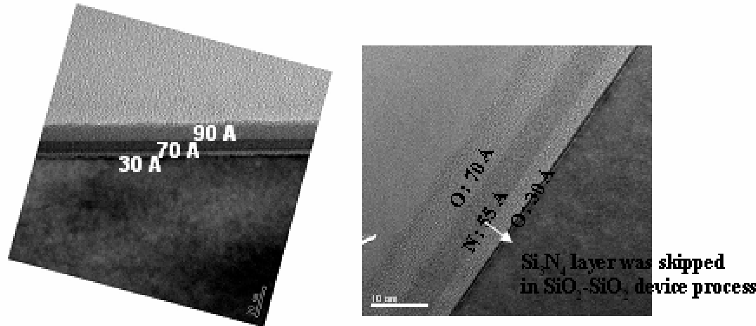


(a) SONOS (b) SiO_2/SiO_2 device

Figure 1. Schematics of (a) SONOS and (b)SiO_2/SiO_2 device and SEM images



(a) SONOS (3/7/9 nm) (b) SiO_2/SiO_2 device (3/7 nm)

Figure 2. TEM images of memory nodes

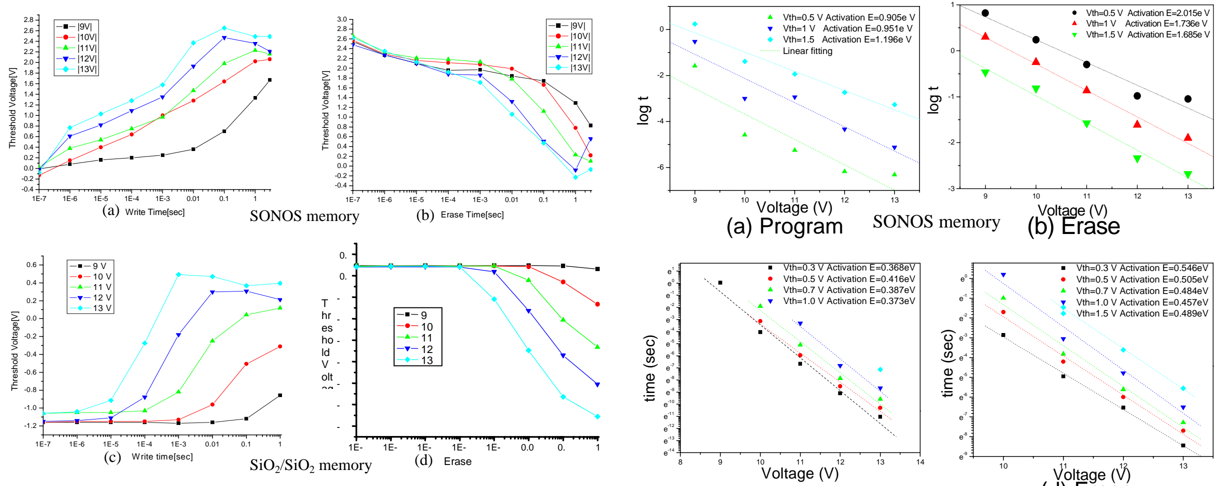


Figure 3. Write(a),(c) and erase(b),(d) characteristics of SONOS(a),(b) and SiO_2/SiO_2 structural device(c),(d)

Figure 4. Activation energy of program/erase process in SONOS and SiO_2/SiO_2 structural device

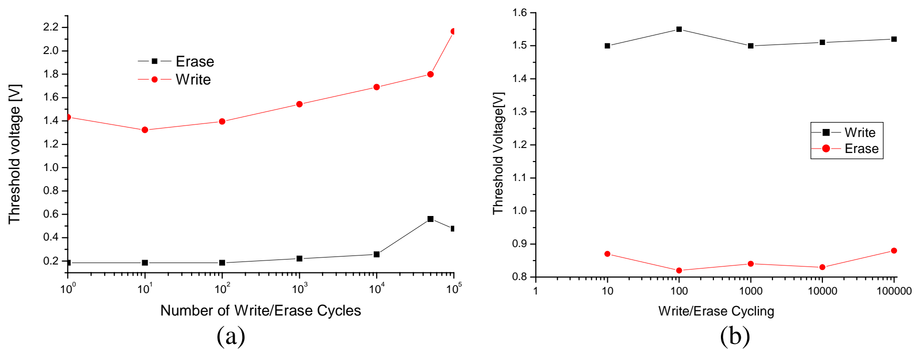


Figure 5. Endurance characteristics of (a) SONOS and (b) SiO_2/SiO_2 device