Realisation of a Novel GaN/ InN Heterostructure FET Device

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Abstract

In this paper we describe the theoretical background, material growth and fabrication process for a novel GaN/InN heterostructure field effect transistor. As proposed by Alexandrov [1], this study into the influence of excitons over the transport phenomena in Wurtzite $In_xGa_{1-x}N$ describes the formation of a conductive channel at the GaN/InN interface. The conductivity of such channel is dependent on the destruction of excitons in their interaction with the GaN – $In_{0.5}Ga_{0.5}N$ interface. Predicted output I-V characteristics of the device are shown in figure 1.

The GaN/InN heterostructure was grown using a remote plasma enhanced CVD process. A 50nm low resistivity InN layer was grown onto a sapphire substrate with a further 50nm of high resistivity GaN. A cross sectional diagram of the proposed device is given in figure 2.

We are currently investigating a two stage lithography process for the fabrication of these devices. Large scale features (typically <100μm) are to be defined through standard photolithography; for example, contact pads, mesa isolation. The small scale structures, namely the Source-Gate-Drain are defined using a Raith 50 electron beam lithography system. An example of test structures of different gate length is shown in figure 3. These features were written into PMMA resist. Following development, a 50nm layer of gold was deposited onto the PMMA; the resultant gold features were defined following lift off. Mesa isolation is defined through dry etching. An Oxford Instruments inductively coupled plasma etching system using BCl_3/Cl_2 chemistry has been used to investigate the etching characteristics of this layer structure. Simple indium metal ohmic contacts are proposed for the Source and Drain. We are currently investigating the possibility of utilising FOx® flowable oxides from Dow Corning in the Gate isolation layer. This material is cured through electron beam exposure.

References

[1] Alexandrov D,*"Excitons of the structure in wurtzite $In_xGa_{1-x}N$ and their properties"*, J. Cryst. Growth, 246, 325-340, (2002)

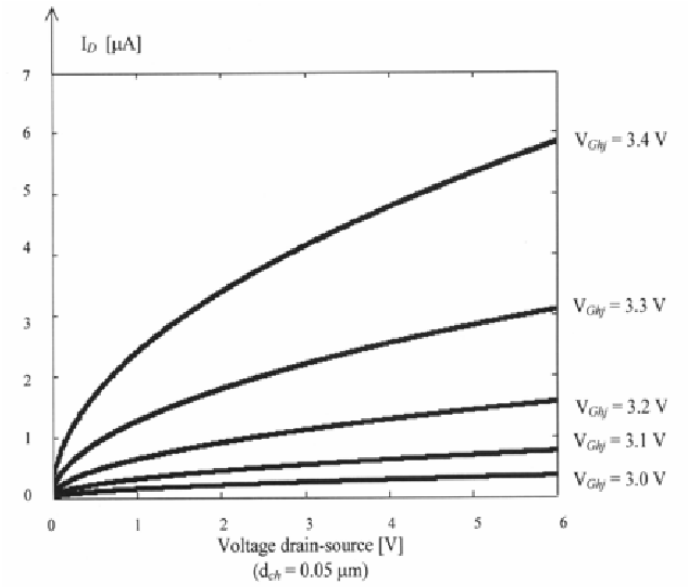

Figure 1: Output current – voltage characteristics of n-channel FET.

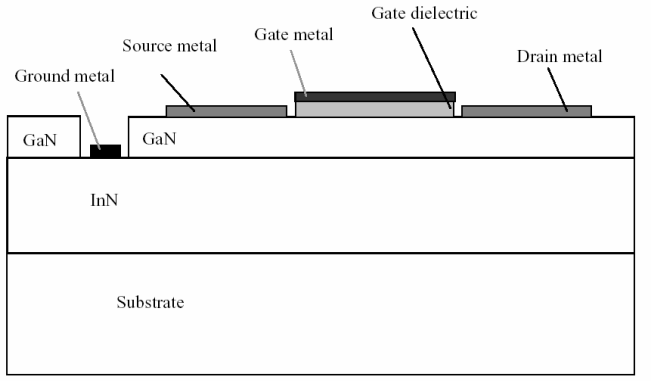

Figure 2: Cross section of the proposed device.

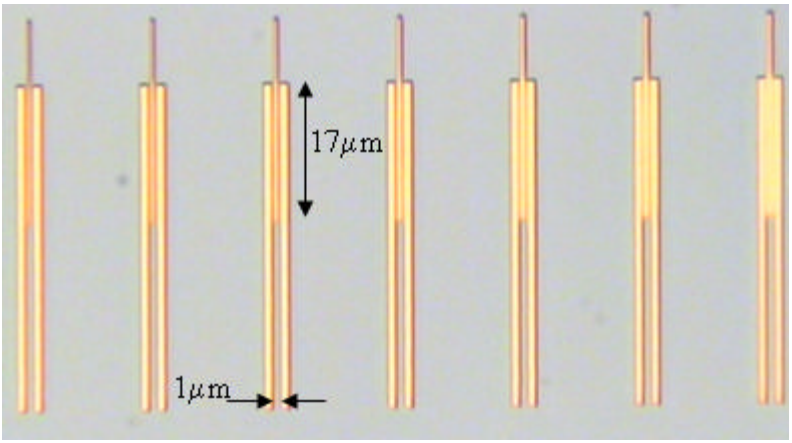

Figure 3: Source-Gate-Drain features defined by electron beam lithography following a gold lift off process.