Optimized Short-Channel SiC Power DMOSFETs with Current Spreading Layers for Low On-Resistance

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SiC DMOSFETs are reaching a level of maturity that will permit their commercial introduction in the near future. In this report, we describe an optimized DMOSFET structure for the 600 to 1,800 V operating regime with extremely low specific on-resistance. The structure makes use of several novel features:(1) a self-aligned short-channel process that produces channel lengths of 300 – 500 nm; (2) a narrow, heavily-doped JFET region; (3) reduced alignment tolerances that minimize cell area; (4) a segmented p+ base contact that reduces the sensitivity of source contact resistance to mask alignment during processing; and (5) a novel n-type current spreading layer (CSL) below the p-base that reduces current crowding into the JFET region.

Device optimization is based on extensive two-dimensional numerical simulations using the MEDICI analysis program. The optimum design point is located in a multi-dimensional parameter space using the Taguchi method. Independent variables in this analysis are drift region doping, CSL doping, JFET region width, and JFET region doping. Our studies indicate that JFET width has the greatest effect on blocking voltage (defined as either avalanche breakdown in the semiconductor or an oxide field in excess of 4 MV/cm), while JFET doping and drift region doping have the greatest effect on specific on-resistance. For a blocking voltage of 1,200 V, the optimum parameters are a JFET width of 1 μm, JFET doping of 1×10^{17} cm^{-3}, CSL doping of 1×10^{17} cm^{-3}, and drift region doping of 1×10^{16} cm^{-3}. For this optimized design, simulations predict a specific on-resistance of 6.9 mΩ cm^2 for the finished device. Experimental devices currently being processed exhibit specific on-resistances as low as 8.3 mΩ cm^2 at probe test prior to contact annealing and top metal.