Charge Trapping and Dielectric Relaxation in Connection with Breakdown of High-k Gate Dielectric Stacks

T. Yuan[a], W. Luo[b], Y. Kuo[c], J. Lu[c], J. Yan[c], S. Chatterjee[c], A. Birge[c], W. Kuo[d]

[a] *Industrial Engineering Dept.*, [b] *Electrical and Computer Engineering Dept.*, [d] *College of Engineering*,

The University of Tennessee, Knoxville, TN 37996

[c] *Thin Films Nano & Microelectronics Research Lab, Texas A&M University, College Station, TX 77843*

Hafnium oxide (HfO_x) is a prospective high-k dielectric to replace conventional gate oxide SiO_2 for ultra-thin gate dielectrics. Doping HfO_x with an appropriate amount of zirconium can improve the k value and reduce leakage. A high-quality interface layer, such as SiO_2 or SiO_xN_y, between silicon substrate and a high-k film is important to the electric and reliability properties of the gate dielectric. However, failure mode and degradation mechanism of stacked structures might be different from that of single-layer dielectric films. When a Zr-doped HfO_x (ZrHfO) film with an interface layer is stressed under gate injection condition, two separate jumps of leakage current are observed at breakdown in addition to the common failure mode of single jump.

Relaxation behaviors and breakdown mechanisms of a variety of nanometer-thick MOS capacitors have been studied. A ramp-relax test is specially designed to monitor polarization/relaxation of these gate stacks. During the test, a negative ramping voltage was applied to the gate. After each ramp step, the bias voltage was switched to a very low voltage for half a second, during which relaxation current was monitored. It is found TiN/ZrHfO/SiO_2/*p*-Si (EOT ~ 2.5 nm) shows a noticeable relaxation current while TiN/SiO_2/*p*-Si (EOT ~ 2.0 nm) does not. The relaxation current signifies the integrity of high-k dielectrics; it disappears at breakdown. This property is used to identify breakdown sequence of two double-layer high-k stacks, TiN/ZrHfO/SiO_2/*p*-Si (EOT ~ 1.8 nm) and Al/Hf-doped TaO_x /silicate/*p*-Si (EOT ~ 1.9 nm). It is identified the interface layer initiates breakdown in the former case, whereas the Hf-doped TaO_x (HfTaO) film collapses first in the latter case. The breakdown sequence is explained with material properties and thicknesses of individual layers. Such information would be valuable in understanding the reliability of multi-layer high-k gate stacks, which is a potential gate dielectric structure for future generations of MOS devices.

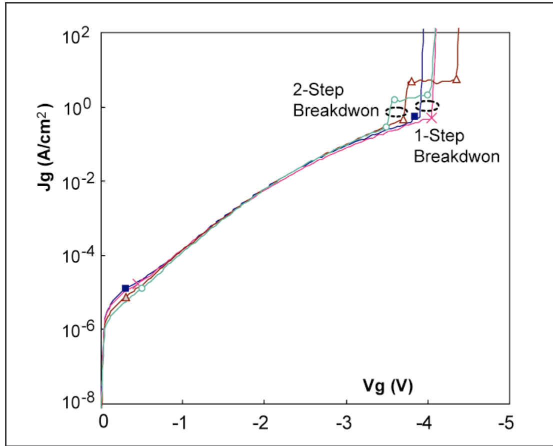

Fig.1. Representative IV characteristics of TiN/ZrHfO /1nm SiO_2/*p*-Si

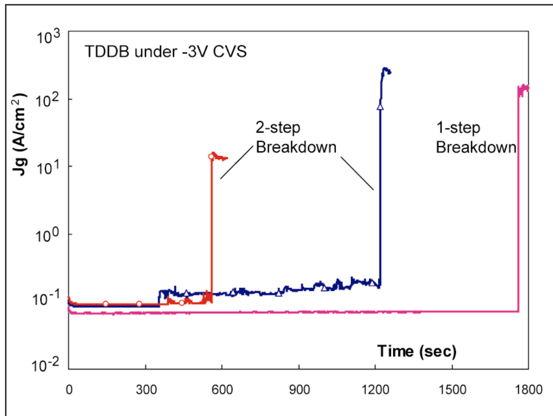

Fig.2. Representative TDDB of TiN/ZrHfO/1nm SiO_2 /*p*-Si

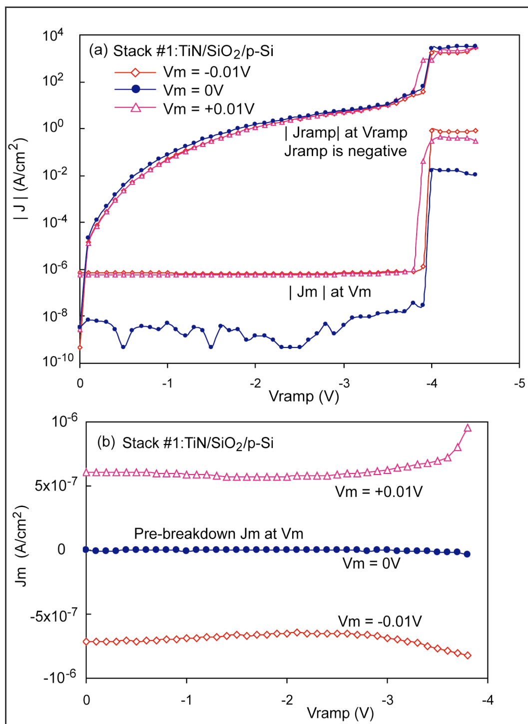

Fig.3. Ramp-relax test on TiN/ZrHfO/2nm SiO_2 /*p*-Si

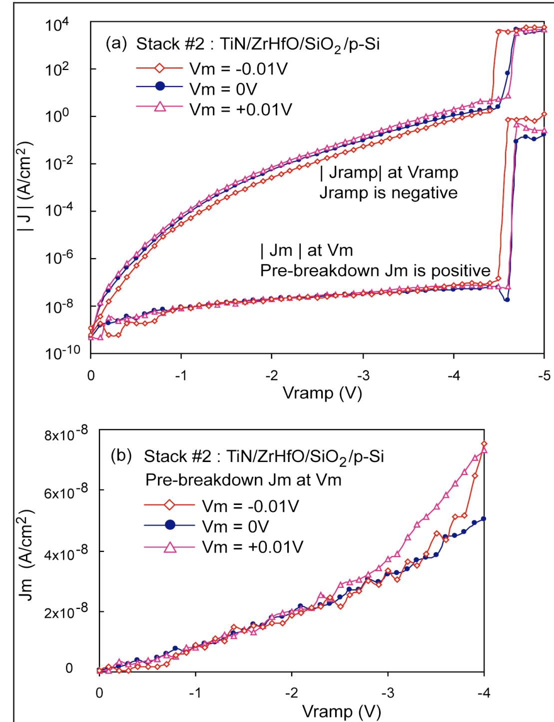

Fig.4. Ramp-relax test on TiN/2nm SiO_2/*p*-Si

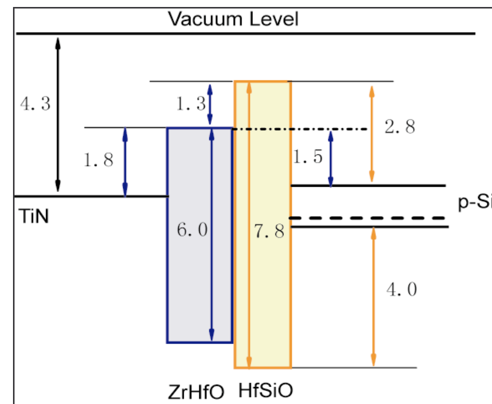

Fig.5. Schematic band diagram of TiN/ZrHfO/1nm SiO_2/*p*-Si

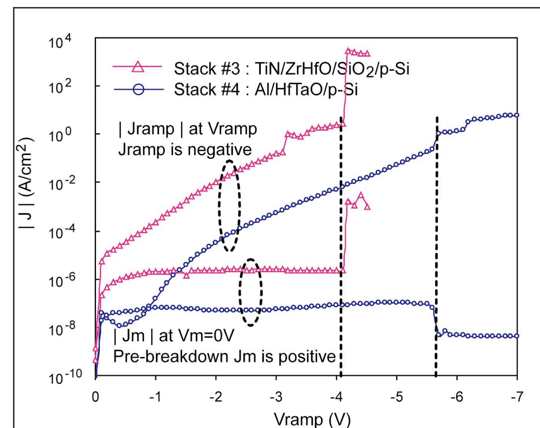

Fig.6. Two-step breakdown mode of TiN/ZrHfO/1nm SiO_2/*p*-Si and Al/HfTaO/silicate/*p*-Si in ramp-relax test