

Negative Bias Temperature Instability in TiN/Hf-silicate Based Gate Stacks

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Hafnium silicate based high- κ gate dielectrics have been put forth as the leading candidates to replace SiO₂ in sub-nm devices in CMOS technology [1]. This work discusses the negative bias temperature instability (NBTI) of TiN/HfSi_xO_y based gate stacks.

HfSi_xO_y (20% SiO₂) was deposited by MOCVD method to fabricate p-channel MOSFETs (Fig. 1) using standard CMOS process flow [2]. PDA in NH₃ was done at 700°C for 60s.

Threshold voltage-shift (ΔV_T) is shown in Fig. 2 for different negative gate bias (V_g) applied on pMOSFETs at room temperature. Mixed degradation due to both electron and positive charge trapping within the bulk oxide under gate injection is most probably responsible for the observed characteristics. We had reported similar results for n-channel devices in our earlier work [3]. Positively charged trap generation within the bulk, induced by hole injection from the substrate at high stress bias, is possible because of the observed correlation between trapping characteristics under constant voltage stress (CVS) and substrate hot hole (SHH) stress conditions (Fig. 3). Trap generation seems to saturate under high bias stress condition at elevated temperature as observed in Fig. 4 although it is found that initially during stress ΔV_T depends on temperature and bias conditions (Fig. 5). Change in sub-threshold swing ($\Delta S/S_0$) was found to be negligible in this case (<5%). Significant interface trap generation (>10%) under high bias and temperature conditions are observed (Fig. 6). Effective mobility at the channel decreases with charge trapping within the bulk high- κ due to coulombic scattering [4]. Hence, $I_{D,SAT}$ and $K_{P,eff}$ ($\approx \mu_{p,eff} C_{ox}(W/L_{eff})$) decrease with temperature and oxide electric field under gate injection (Fig. 7).

Positive charge trapping was found to be thermally activated with activation energy (E_a) in the range of 0.2-0.3 eV (Fig. 8). E_a due to H-species diffusion in SiO₂ is 0.1-0.2 eV, whereas due to H-species hopping in HfO₂ is calculated to be 0.8 eV [5]. Therefore, we believe initially during stress, Si-H bond breaking could probably occur at the interface under bias and at the presence of substrate holes. H-species diffuse through SiO₂ interfacial layer (IL) and diffuse and/or hop across the bulk Hf-silicate (20% SiO₂) at elevated temperature, and thus induce positive charge trapping within the gate stack. Post-stress injection of substrate electrons (Fig. 9) fails to neutralize $|\Delta V_T|$, which further suggests that H-species are probably responsible for positive charge trapping [5].

D_{it} is high ($\approx 8 \times 10^{12}$ cm².eV⁻¹) in our fresh devices as interfacial layer (IL) is chemically grown SiO₂ [2]. Hence, $\Delta S/S_0$ was observed to be low and the availability of H-species due to Si-H bond breaking is limited. Use up of H-species was reported to limit increase of ΔV_T [6]. H-passivated E' centers (H-Si≡O), observed in chemically grown IL [7], may be another potential source of H-species during gate injection. Therefore, shortage of available H-species is possibly responsible for saturation of ΔV_T at elevated temperatures under negative bias stress conditions.

In summary, mixed degradation due to electron and positive charge trapping within the bulk dominates for low negative gate bias at room temperature under CVS, whereas for high bias conditions bulk trap generation occurs. Initial positive charge trap generation within the gate stack and at the interface under bias and elevated temperature conditions, which is responsible for increased $|\Delta V_T|$ and decreased $\mu_{p,eff}$ and $I_{D,SAT}$, is found to saturate. H-species are probably responsible for the observed NBTI effects.

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References:

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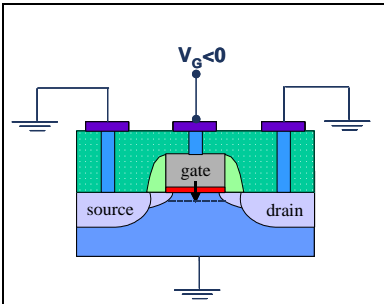


Fig.1. Set-up for studying NBTI effects. CVS with $-ve$ bias is applied on pMOSFET at different temperatures while gate, source, drain and substrate currents are measured.

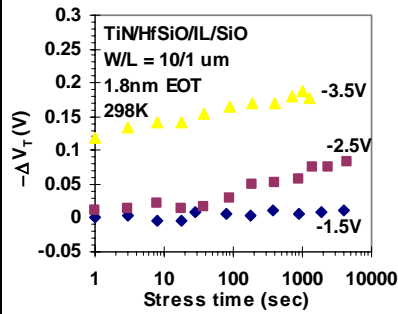


Fig.2. Threshold voltage shift ($-\Delta V_T$) for different $-ve$ gate bias at room temperature. Mixed degradation due to electron and $+ve$ charge trapping within the bulk oxide dominates for low bias, whereas trap generation occurs for high bias.

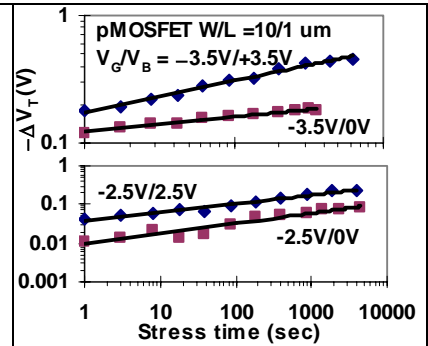


Fig.3. $-\Delta V_T$ under subs. hot hole (SHH) stress and CVS conditions. Correlation between trapping characteristics is observed. Hole injection from substrate induces positive charge trap generation.

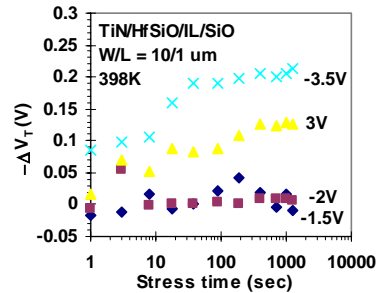


Fig.4. $-\Delta V_T$ for different $-ve$ gate bias at elevated temperature. Mixed degradation is significant for low bias. For high bias, initial trap generation is followed by saturation in $+ve$ charge trapping.

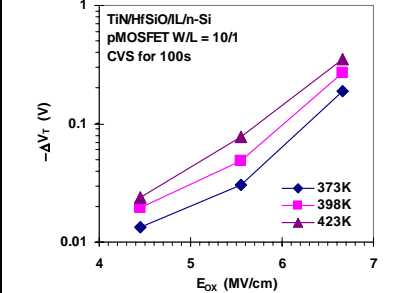


Fig.5. $-\Delta V_T$ after 100s of CVS at different stress electric field ($E_{ox} = (V_g - V_{FB} - \psi_s)/t_{ox}$) and temperature conditions. Significant $+ve$ charge trap generation under gate injection is obvious.

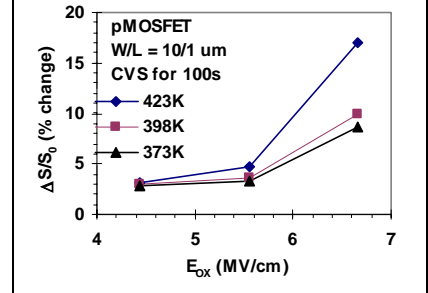


Fig. 6. Change in normalized subthreshold swing ($\Delta S/S_0$) after 100s of CVS at different stress electric field and temperature conditions. Interface state generation is significant at high bias and elevated temperature conditions.

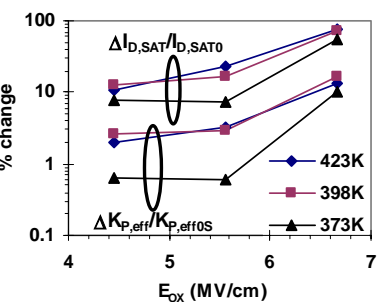


Fig. 7. Normalized Change in $I_{D,SAT}$ and K_P after 100s of CVS at different stress electric field and temperature conditions.

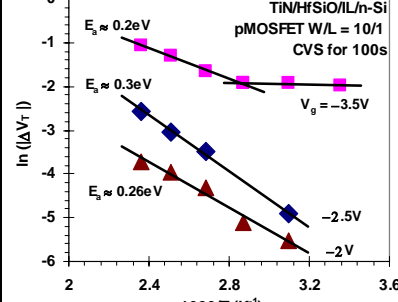


Fig. 8. Arrhenius plot of $|\Delta V_T|$ after 100s of CVS at different $-ve$ gate bias. Activation energy (E_a) of $+ve$ charge build-up is in 0.2-0.3 eV range.

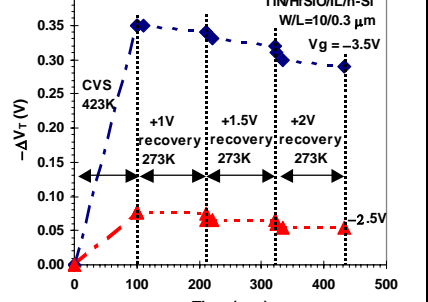


Fig. 9. Post-stress substrate electron injection after CVS at high $-ve$ bias and elevated temperature conditions. Negligible recovery suggests H-species induced $+ve$ charge trap generation.