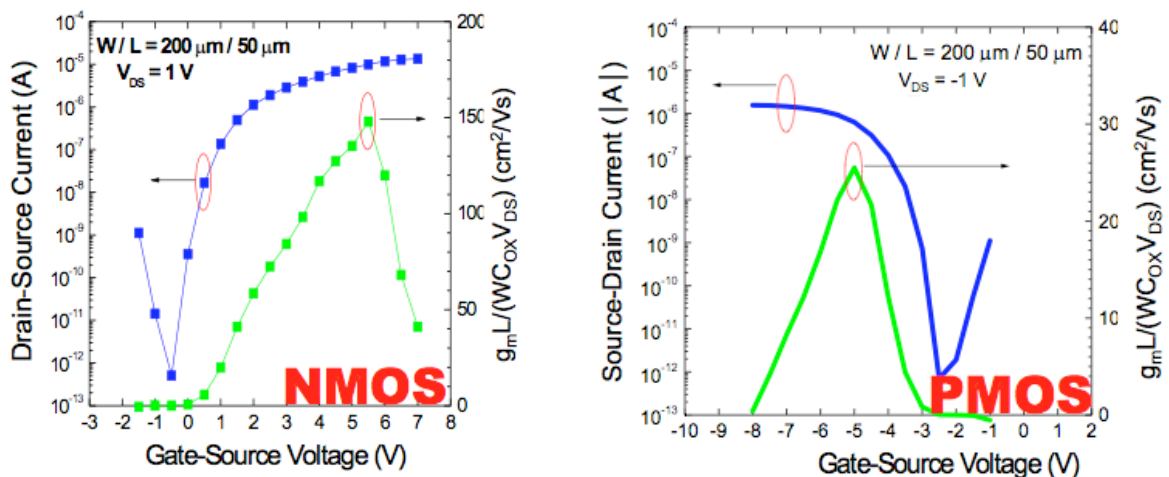


## Nanocrystalline Silicon Thin Film Transistors

Arokia Nathan<sup>1</sup>, Andrei Sazonov, Czang-Ho Lee, John Robertson<sup>2</sup>  
Electrical and Computer Engineering, University of Waterloo, Waterloo, Canada  
<sup>1</sup>Visiting Professor, <sup>1,2</sup>Electrical Engineering Division, University of Cambridge, UK

The evolution in materials and process fabrication technologies is posing new challenges and application areas in large area electronics. A driving force in this evolution is silicon thin film technology. Interest in thin film silicon extends well beyond the active matrix liquid crystal display and stems from a variety of desired technological features including low temperature manufacturing with few constraints on the substrate size, material, or topology. More recently, the extension of the technology to plastic substrates has received considerable attention. Interests on plastic is being driven by the need for lightweight, unbreakable, and eventually foldable screens for displays and imagers, along with a plethora of new generation applications ranging from media to bio-medicine.

Because of material structure thin film silicon does not enjoy the same electronic properties, such as speed and current drive capability compared to crystalline Si. However, it is currently being challenged with new material and device structures for high performance. For example, high-current drive capability of thin-film transistors (TFTs) is a critical requirement for system-on-panel integration of switching devices and peripheral circuit drivers in flat panel imagers and displays. Although laser-annealed polycrystalline silicon (poly-Si) TFTs are used for such applications, they suffer from high manufacturing cost, complex processing, and non-uniformity of electronic performance over the panel area. While high-performance nanocrystalline silicon (nc-Si:H) directly deposited at low substrate temperature is a promising candidate, attempts to fabricate such a device have been met with limited success. Furthermore, to realize the building blocks pertinent to complementary digital circuits, high performance p-channel TFTs are needed. Hole mobilities reported to date for nc-Si:H TFTs are in the range  $\sim 0.25$   $\text{cm}^2/\text{Vs}$ , but these values are still very small compared to the poly-Si counterpart ( $\sim 100$   $\text{cm}^2/\text{Vs}$ ). This talk will describe high transconductance nanocrystalline silicon (nc-Si:H) top-gate staggered thin-film transistors (TFTs) fabricated by radio-frequency plasma-enhanced chemical vapor deposition (RF-PECVD) at low temperatures. Nanocrystalline silicon TFTs show a normalized transconductance or effective field-effect electron mobility of  $150$   $\text{cm}^2/\text{Vs}$ , and an effective hole mobility of  $25$   $\text{cm}^2/\text{Vs}$  (see Fig. 1). To the best of our knowledge, the values reported here are the highest achieved to date using RF-PECVD.



**Fig.1** Top-gate nanocrystalline silicon thin film transistor transfer characteristics. Effective device mobilities are  $150$   $\text{cm}^2/\text{V-s}$  and  $25$   $\text{cm}^2/\text{V-s}$  for n-channel and p-channel transistors, respectively.