N-face High Electron Mobility Transistors with a GaN spacer

Man Hoi Wong[1], Siddharth Rajan[1], Rongming Chu[1], Tomás Palacios[1], Chang-Soo Suh[1], Lee S. McCarthy[1], Stacia Keller[1], James S. Speck[2] and Umesh K. Mishra[1]
[1] Electrical and Computer Engineering and [2]Materials Departments
University of California, Santa Barbara, CA 93106, USA
Email: mhwong@ece.ucsb.edu / Phone: +1-805-893-3812/ Fax: +1-805-893-8714

Strong confinement of the two-dimensional electron gas (2DEG) in nitride high electron mobility transistors (HEMTs) is critical for good pinch-off and output conductance under high electric fields. In Ga-polar (0001) AlGaN/GaN HEMTs a successful approach is the use of thin InGaN back barriers where polarization engineering is used to enhance 2DEG confinement [1]. N-polar (000-1) GaN/AlGaN/GaN HEMTs offer the advantage of a natural barrier for electrons under reverse bias since electric fields induced by the reversed polarization push the electrons towards the AlGaN back barrier [2,3,4]. However, transport properties degrade due to strong scattering from the AlGaN random alloy. Here we present an N-face HEMT using an ultrathin AlN interlayer between a GaN spacer and the GaN channel, which provides very strong 2DEG confinement with low alloy scattering. Higher effective electron velocity has been obtained in Ga-face HEMTs with a GaN spacer [5].

The N-face GaN spacer HEMT is based on a GaN/AlN/GaN heterojunction to confine the 2DEG [6] (Fig. 1). The polarization-induced conduction band discontinuity, ΔE_P, between the two GaN layers is proportional to the AlN thickness. The large polarization of AlN ($\Delta E_P \sim 1.3$ eV/nm) enables the use of an ultrathin layer for excellent confinement with minimal impact on transport. Si δ-doping is inserted below the AlN to provide charge for the channel and to prevent modulation of hole traps close to the valence band at the GaN/AlN interface [3,7].

All devices were grown by plasma-assisted MBE on C-face 6H-SiC substrates at 720 °C. A two-step GaN buffer was used to reduce threading dislocation density to the low 10^{10} cm^{-2} [2]. A 24 nm digital AlGaN layer helped induce charges in the channel, followed by a 4 nm GaN spacer, 2 nm AlN interlayer and 15 nm channel layer. The devices were capped by 20 nm $Al_{0.1}Ga_{0.9}N$ to increase the breakdown voltage [4] (Fig. 2). HRXRD confirmed the good structural and buffer qualities. Typical full-width half-maximum of rocking curves taken in the symmetric on-axis (000-2) and off-axis (20-2-1) skew geometries were 0.13° and 0.35° respectively.

A 4 nm SiN_x insulator was deposited by MOCVD prior to processing to suppress gate leakage. Devices were fabricated with Ti/Al/Ni/Au (20/100/10/50 nm) Ohmic metallization, annealed at 870°C for 30 sec in N_2 atmosphere. Mesas were etched with Cl_2-based plasma. Ni/Au/Ni metallization was used for the gates. The surface was subsequently passivated with SiN_x deposited by PECVD. All devices were 2x75 µm wide with 0.7 µm nominal gate length and 0.7 µm gate-source spacing. The Ohmic spacing was 3.4 µm.

Room temperature 2DEG density was 7×10^{12} cm^{-2} with Hall mobilities ranging from 1550 to 1750 cm^2/Vs, which were 20% higher than in N-face HEMTs without the AlN interlayer [4]. DC-IV and capacitance-voltage (*CV*) measurements exhibited sharp pinchoff. The maximum drain current I_{max} was 0.73A/mm at V_G = +1V. Off-state breakdown at 1 mA/mm was in excess of 55V (Fig. 3). Current-voltage measurements under pulsed conditions with the device biased on a 50 Ω load line indicated a limited amount of DC-RF dispersion (Fig. 4).

Small signal *s*-parameter measurements were performed with an Agilent E8361A network analyzer. A maximum f_t of 24 GHz and f_{max} of 44 GHz were achieved at I_{DS} = 267 mA/mm and V_{DS} = 15V. Power measurements were performed using a Maury microwave load-pull system. Measurements at 4 GHz with a drain bias of 40V and quiescent current of 293 mA/mm yielded a transducer gain G_T of 10.3 dB and maximum output power density P_{out} of 4.5 W/mm with power added efficiency (PAE) of 34% (Fig. 5).

In summary, N-face GaN transistors with the use of a GaN spacer and ultrathin AlN layer for extra electron confinement has been realized. Lower alloy scattering has led to significant improvements in mobility. With improved growth and processing technologies for reducing gate leakage as well as preventing dispersion due to surface and interfacial hole traps, power capability in N-face transistors was demonstrated. N-face materials are therefore promising for high-frequency and high-power electronic devices.

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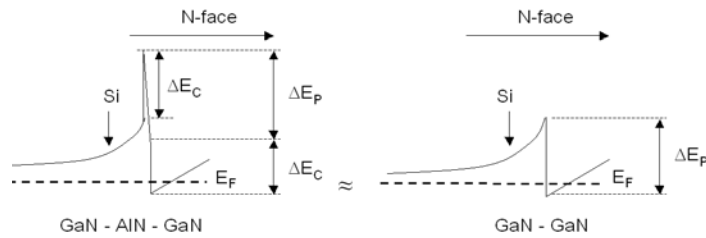
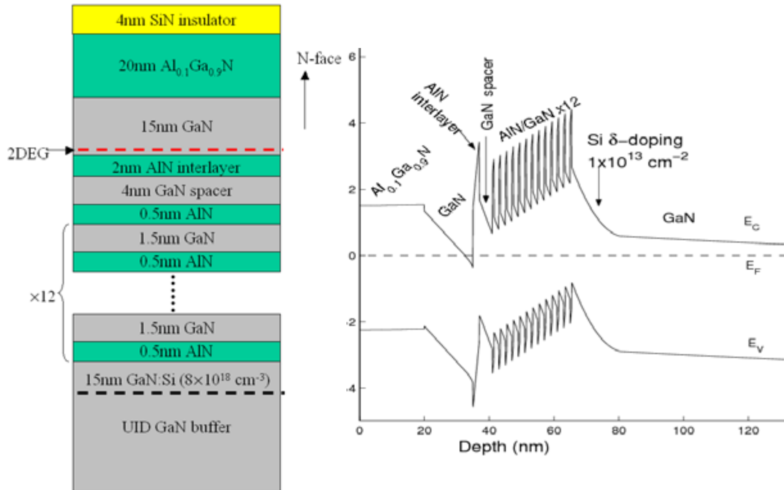


Fig. 1 GaN/AlN/GaN heterojunction



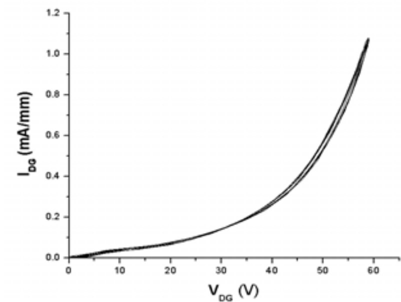


Fig. 2 Schematic and band diagram of the N-face GaN spacer HEMT

Fig. 3 Two-terminal GD leakage at 1mA/mm was in excess of 55V

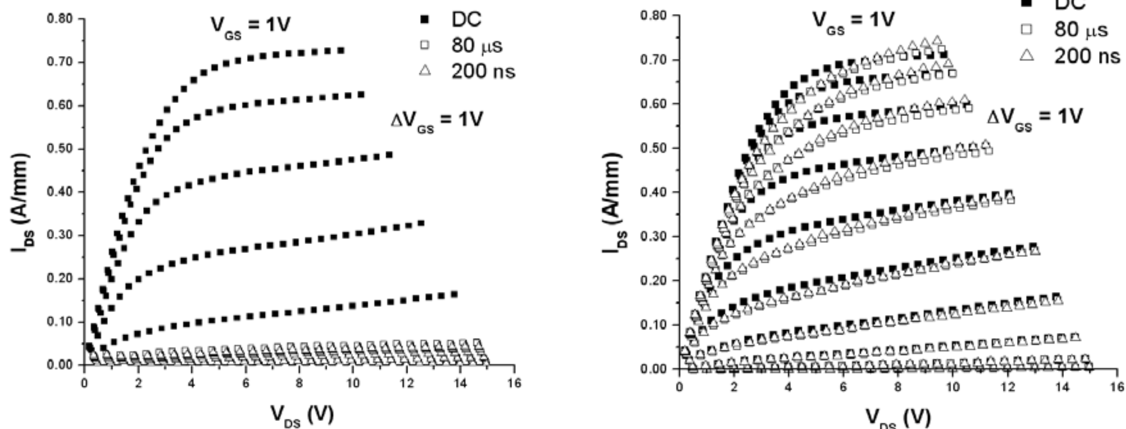


Fig. 4 DC and pulsed-IV (80 µs and 200 ns pulse-widths) measurements at $V_{DS,max}$ = 15V Left: Before passivation; Right: After SiN_x passivation

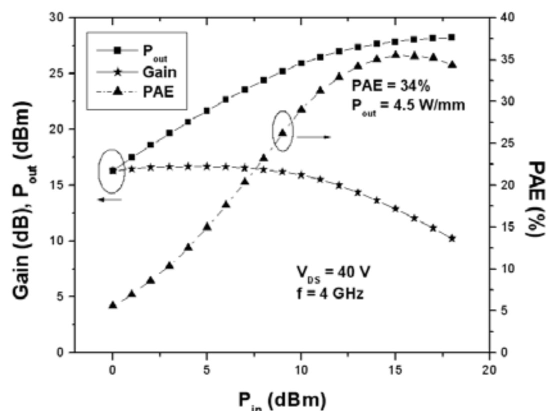


Fig. 5 Load-pull power measurement of N-face GaN spacer