Simulations of gate-recessed and field-plated AlGaN-GaN heterojunction field-effect transistors

Valentin O. Turin, Michael S. Shur
Department of Electrical, Computer and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY 12180 USA
E-mails: touriv@rpi.edu, shurm@rpi.edu

Dmitry B. Veksler,
Department of Physics, Applied Physics and Astronomy, Rensselaer Polytechnic Institute, Troy, NY, 12180, USA
E-mail: veksld@rpi.edu

ABSTRACT

Over the past several years, GaN-based field-effect transistors have demonstrated potential for high-voltage and high microwave power applications. However, their reliability still limits their applications in today's electronic systems. The newly developed deep-submicrometer gate-recessed and field-plated AlGaN-GaN heterojunction field-effect transistors (HFETs) show improved performance due to the electric field reduction in the device channel and surface modification. We report on two-dimensional simulations of gate-recessed and field-plated AlGaN-GaN HEMTs with submicron gates that provide insight into the device physics and allow for the design optimization. The simulations were performed using commercially available SDEVICE TCAD software from SYNOPSYS, Inc. We ran isothermal simulations of output and transfer characteristics in the frame of drift-diffusion model and compared the HFET designs with and without field plate as well as the conventional gate and recessed gate designs. In addition, we have simulated gate with facet on its drain side for different recess angles. Such recessed gate design with a field plate shows the lowest field value at the drain-side gate edge and the most uniform field distribution in the channel. For the recessed 150 nm gate with the 45^0 recess angle and with 60 nm field plate the maximum field in the channel was about 40% less compared to the conventional gate. Cut-off frequency dependence on drain-source bias was studied for all considered gate designs. Simulations show a dramatic increase of the effective length of the gate with increasing drain-source bias. A commensurate decrease of the cut-off frequency with rising drain-source voltage was observed in the simulations (up to 40% decrease for 50V). To improve the cut-off frequency for the high drain-source bias, we suggest to use the second long field plate connected to the drain. Simulations show that the field distribution between the gate edge and the edge of the drain field plate is similar to the dipole field distribution. In this case, the high field remains localized in the gap between the gate and drain field plate without a significant increase of the effective length of the gate. For such a design, the cut-off frequency was dramatically improved for high drain-source biases (with only 8 % decrease for 50V). The obtained results might be useful for transistor design optimization and improvement.

EXTENDED ABSTRACT

Presented figures and table are complementary to the main abstract text.

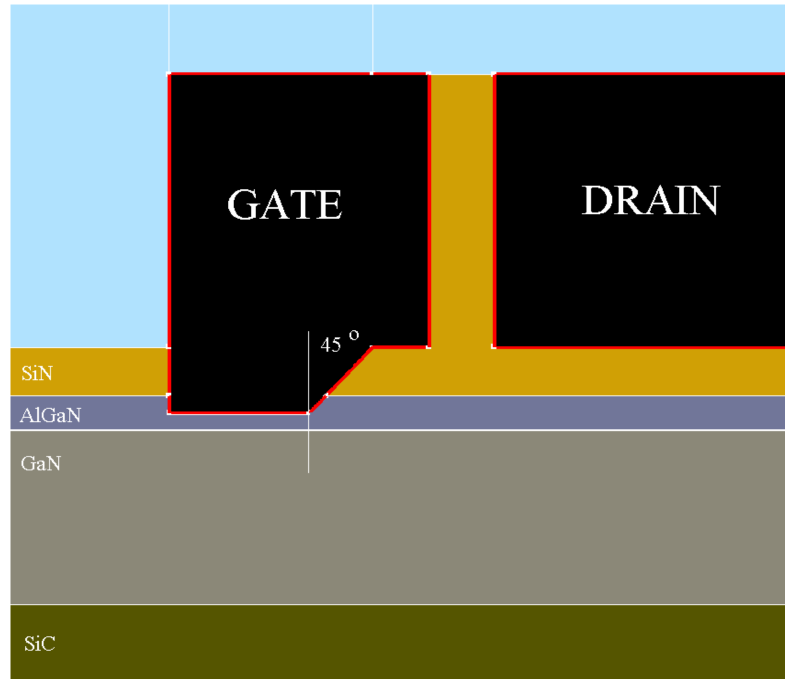
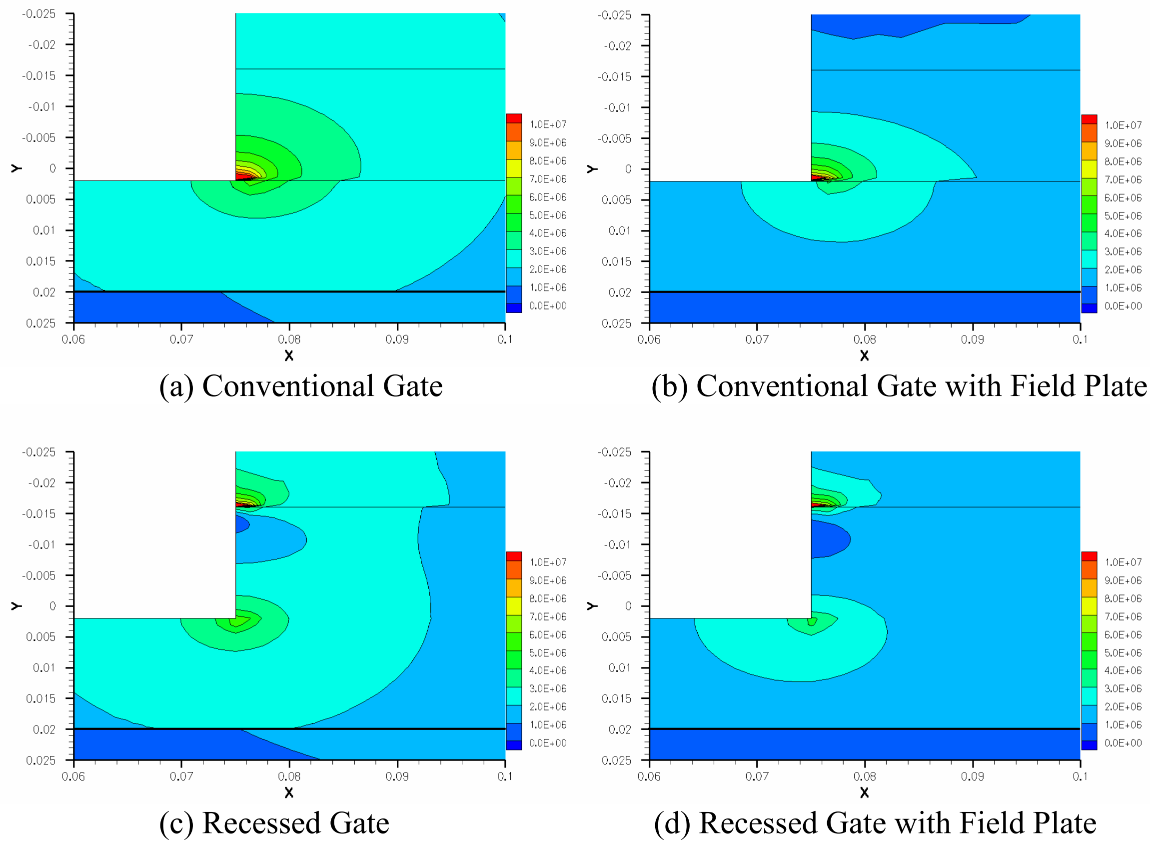


Fig. 1: Schematic of considered field-plated HFET with recessed faced gate with field plate connected to gate and with second long field plate connected to drain.

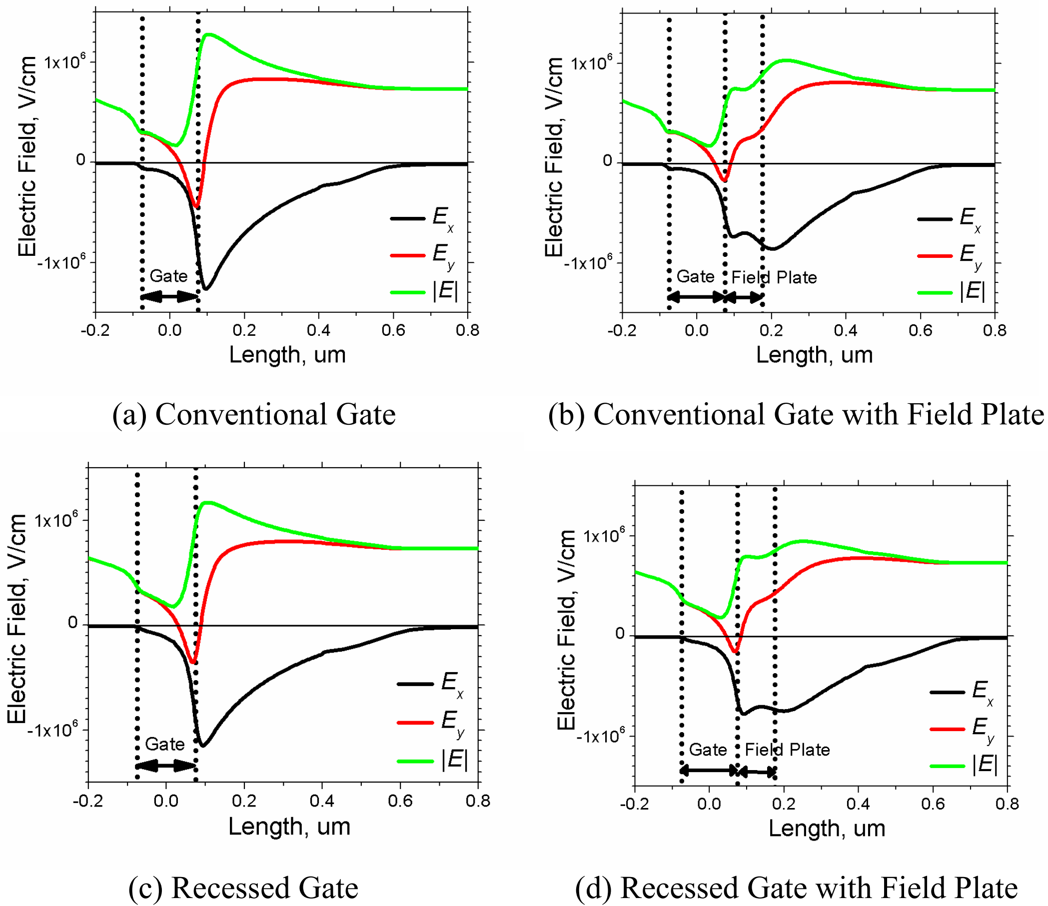
In Figure 1 SiN passivation thickness is 50 nm. Gate length is 0.15 µm. Field plate length is 60 nm. Channel thickness is 18 nm. Recessed gate depth is 18 nm. Facet angle is 45^0. Gap between field plates is 70 nm. Source-drain distance is 3.8 µm. Source-gate distance is 0.925 µm. Electron mobility is 1200 cm^2/Vs. Electron saturation velocity is 2×10^7 cm/s.



(a) Conventional Gate (b) Conventional Gate with Field Plate

(c) Recessed Gate (d) Recessed Gate with Field Plate

Fig. 2: Electric field (V/cm) distribution at the drain-side of gate for the cases with and without field plate for both conventional and recessed gate designs. Source-to-gate bias is zero; drain-source voltage is 30 V.



(a) Conventional Gate

(b) Conventional Gate with Field Plate

(c) Recessed Gate

(d) Recessed Gate with Field Plate

Fig. 3: Electric field (V/cm) distribution in the HEMT channel (1 nm below AlGaN–GaN interface) for the case of: (a) conventional gate design, (b) field plated gate, (c) recessed gate, (d) recessed gate with field plate.

Figure 2 shows the 2D distribution of the electric field at the drain side of the channel. As seen, in case of the recessed gate, electric field has two maxima: at the gate edge and at the AlGaN/SiN interface, accordingly. This allows reducing the electric field strength in the vicinity of the gate edge. Combination of the field termination plate (100 nm) with the gate recession makes the field distribution in the channel more uniform (see Fig. 3). This improves the breakdown characteristics of the device.

The effective length of the gate to be estimated as follows:

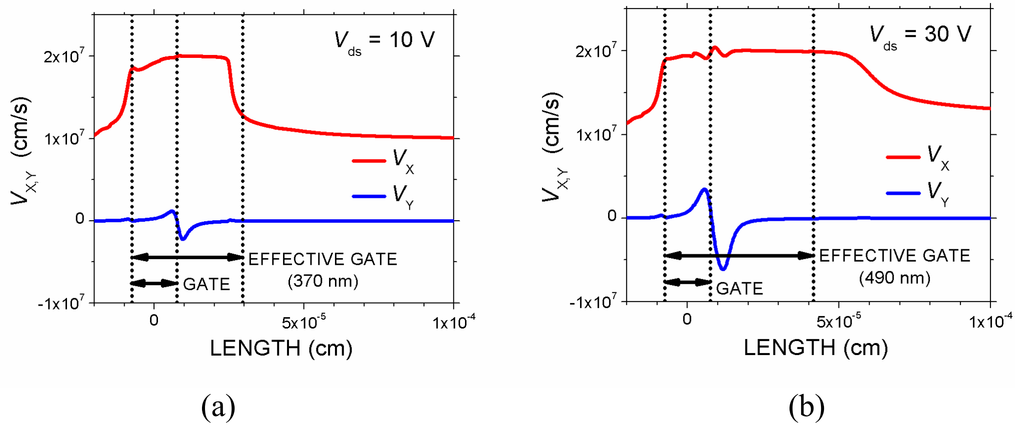
$$L_{geff} = \frac{v_{sat}}{2\pi f_t}$$

Table 1 shows the effective lengths values for different drain-source voltages for the conventional gate design. The data for f_t are extracted form simulations (see Fig. 9).

Table 1:

	V_{sd} = 10 V	V_{sd} = 30 V
f_t, GHz	86	65
L_{geff}, nm	370	490

Data for the L_{geff} are presented in the Fig. 4 together with the simulated velocity profiles. From Fig. 4, one should notice that the gate effective length increases with increasing drain-source bias. The effective length extracted from the cut-off frequency simulations is in a good agreement with the length of the velocity saturation region in the channel.



(a) (b)

Fig. 4: Distribution of electron velocity in the channel under the gate (1 nm below AlGaN/GaN interface) for the case of a conventional gate design at zero drain-gate bias. Gate length is 0.15 µm. (a) V_{ds} = 10 V, (b) V_{ds} =30 V.

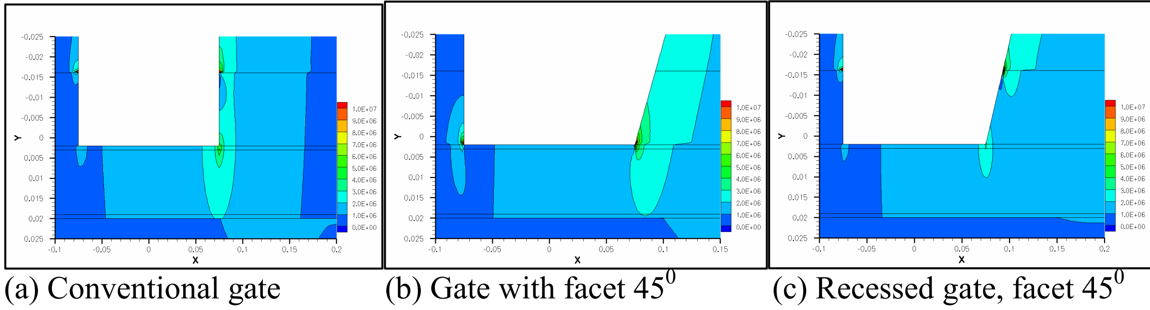


Fig. 5: Electric field (V/cm) distribution under gate for the cases of (a) conventional gate, (b) gate with 45^0 facet, and (c) for recessed gate with 45^0 facet. Source-to-gate bias is zero; drain-source voltage is 30 V.

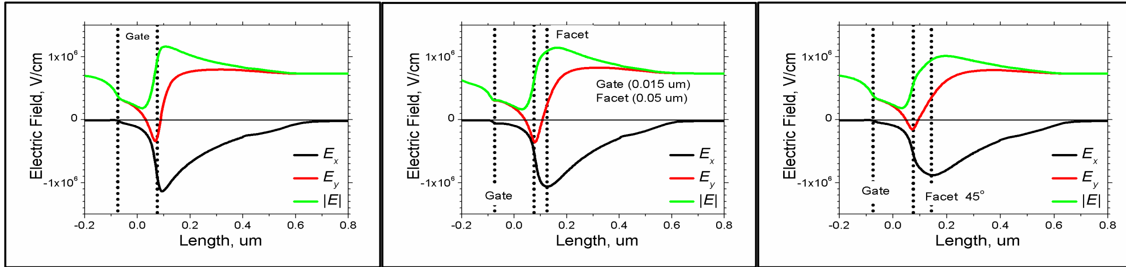


Fig. 6: Electric field (V/cm) distribution in the HEMT channel (1 nm below AlGaN–GaN interface) for the case of: (a) conventional gate, (b) gate with 45^0 facet, and (c) for recessed gate with 45^0 facet.

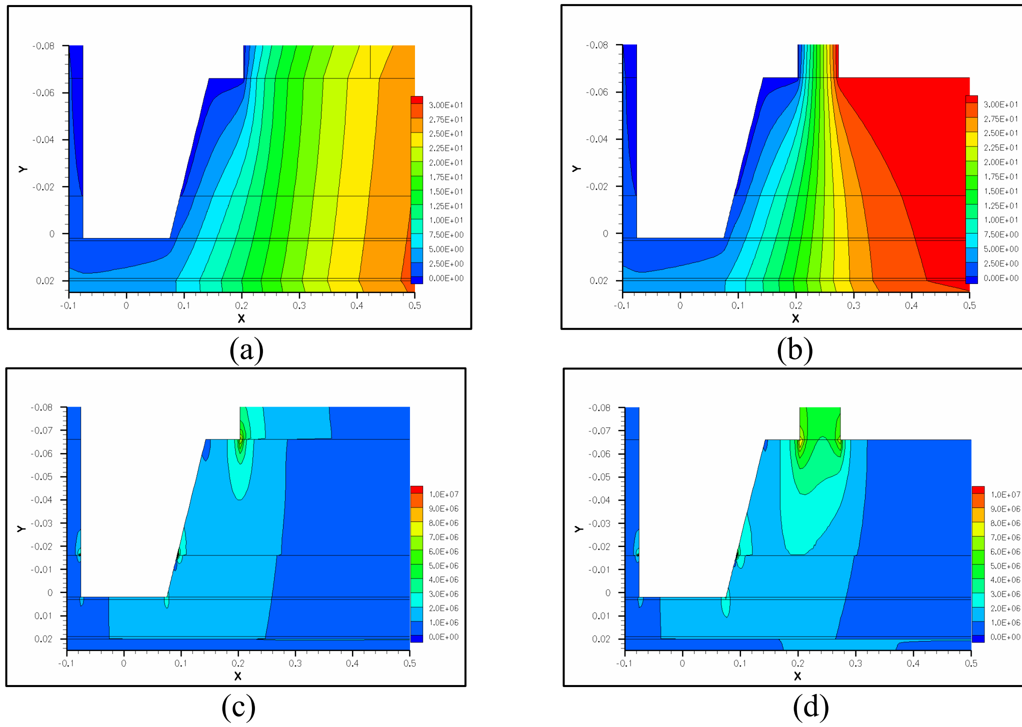


Fig. 7: Potential distribution (V) at the gate edge for the case of without second field plate (a) and for the case with long second field plate connected to drain (b). (c) and (d) is the field distribution (V/cm) for both cases. On (d) there is a clear view of the dipole-type field distribution.

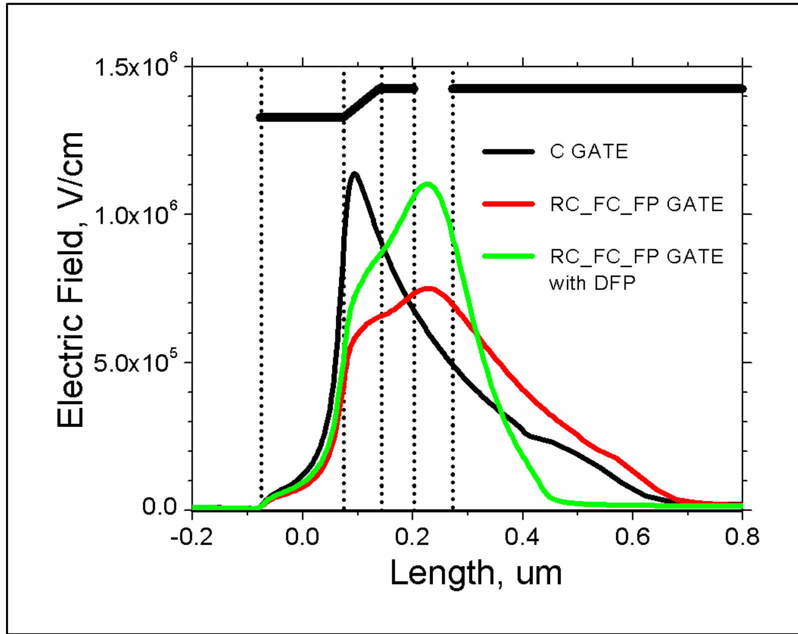


Fig. 8: Field distribution (V/cm) 1 nm under AlGaN/GaN interface for conventional gate (black line), recessed gate with 45^0 facet and with field plate connected to gate (red line), and recessed gate with 45^0 facet and with first field plate connected to gate and second to drain.

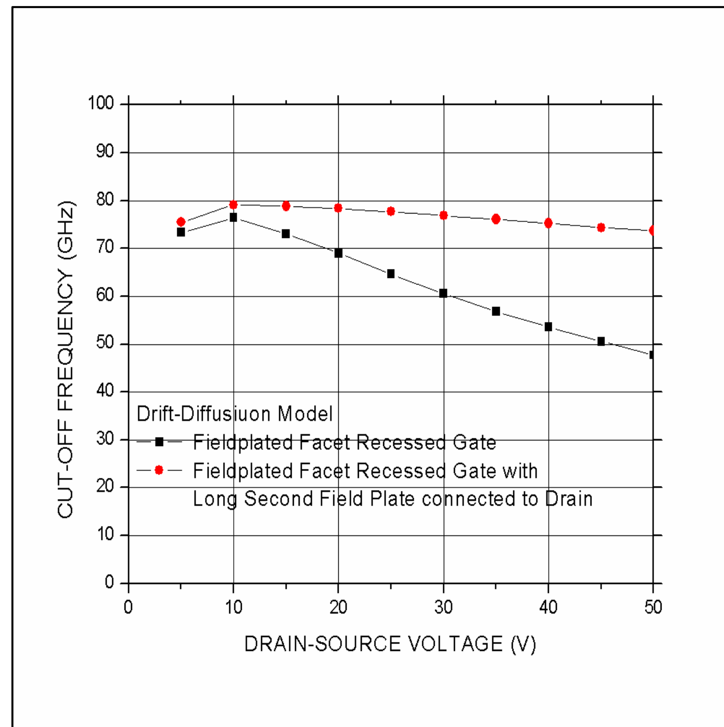


Fig. 9: Cut-off frequency dependence on drain-source voltage for HFET with field-plated recessed gate with 45^0 facet and for the same gate with second long field-plate connected to drain.

Figure 9 shows the cut-off frequency versus the drain-source voltage for two different gate designs. One can notice the decrease of the HFET cut-off frequency with increasing drain-source bias for the case without second field plate. To improve cut-off frequency for high drain-source bias we suggest to use second long field plate connected to drain. Simulations show, that the gate edge and the edge of such a field plate forms field distribution similar to dipole has. In this case, the high field is localized in the gap between gate and second field plate without a significant increase of the effective length of the gate. For such a design, the cut-off frequency was dramatically improved for high drain-source biases (only 8 % decrease for 50 V drain-source bias). The obtained results might be useful for transistor design optimization and improvement.

Related references:

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